



2012 Open Innovation Platform[®]

ECOSYSTEM FORUM

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EDA / IP / Services Track

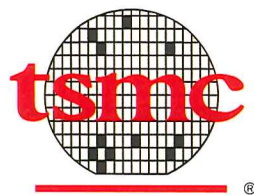
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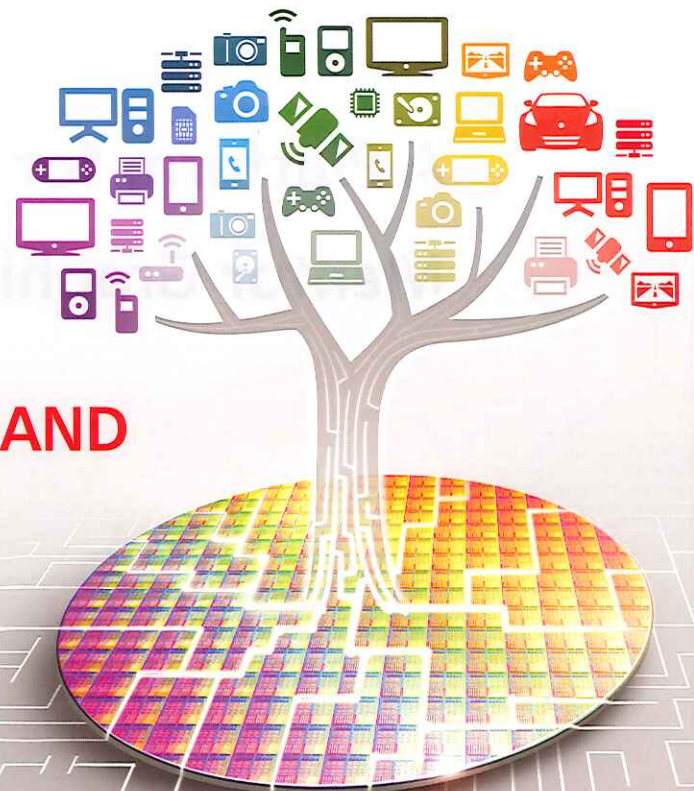
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EDA Track

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A Platform for the CoWoS™ Reference Flow

Mentor Graphics



ABSTRACT

The first phase of 3D-IC adoption will be based on silicon interposers. Designing multi-die systems using this technology introduces new challenges for the EDA design flow.

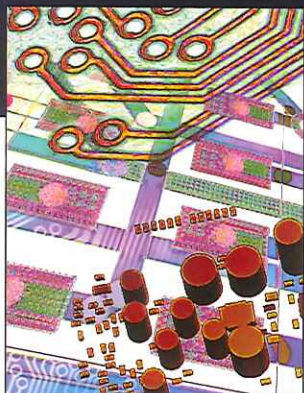
This session will provide an overview of the key challenges of 3D-IC at the planning, optimization, implementation, verification, and test stages of the design flow. We will also describe how EDA tools are being extended to address these issues:

- Planning, assembling and optimizing interposer-based designs
- P&R support for TSV, microbumps, silicon interposer redistribution layer (RDL) and signal routing
- Multi-die integration and the need for a 3D-IC cockpit
- New extraction challenges and modeling of silicon interposers and through silicon vias (TSVs)
- Test infrastructure insertion to support test access to die test features within the package
- Testing TSVs, interposers and inter-die connections, and reusing die patterns after packaging

We will also hint at the future roadmap for IC/package co-design and the evolution to integrated IC, package and PCB design environment to enable true “vertical scaling.”



A Platform for the CoWoS™ Reference Flow

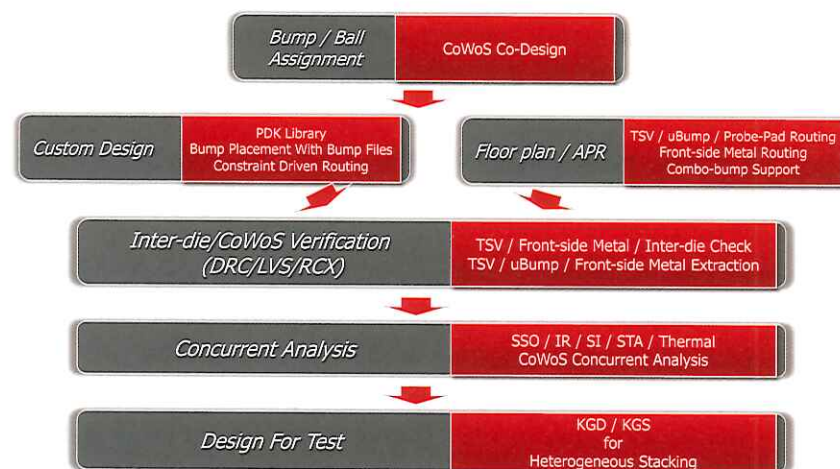


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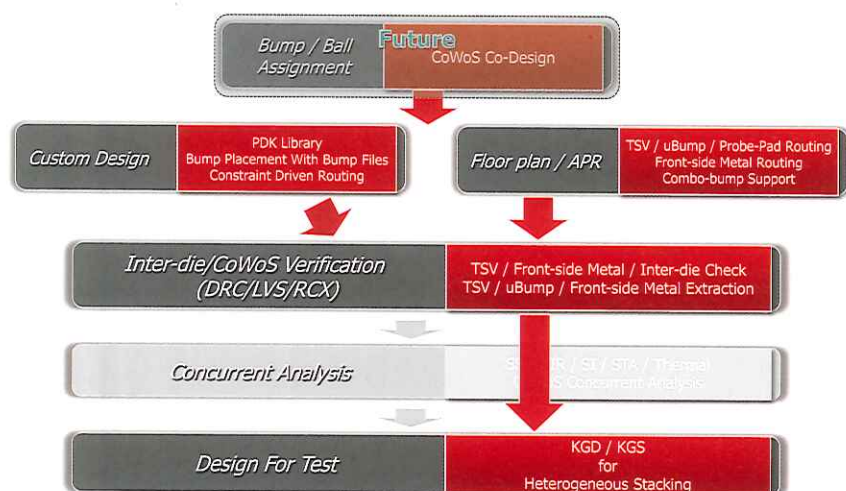
John Park
Methodology Architect



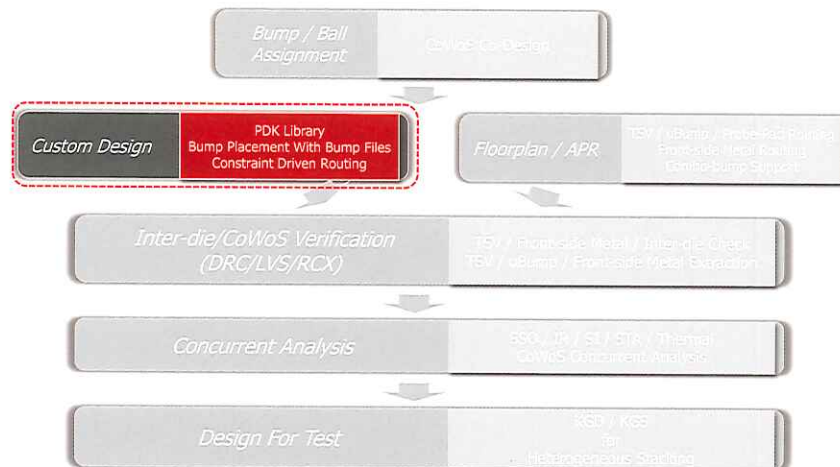
TSMC CoWoS™ Reference Flow Design Solutions



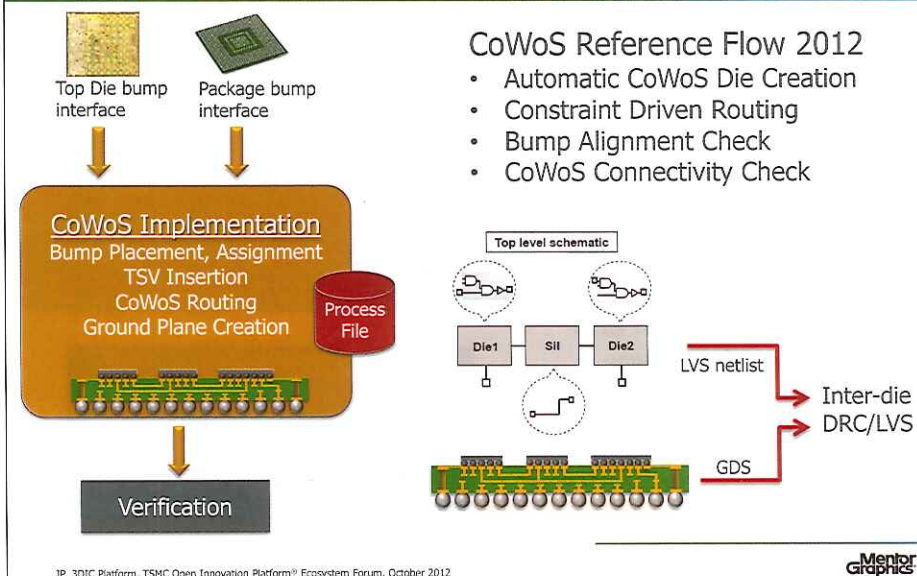
Outline Mentor Graphics® Solutions, Today and Future...



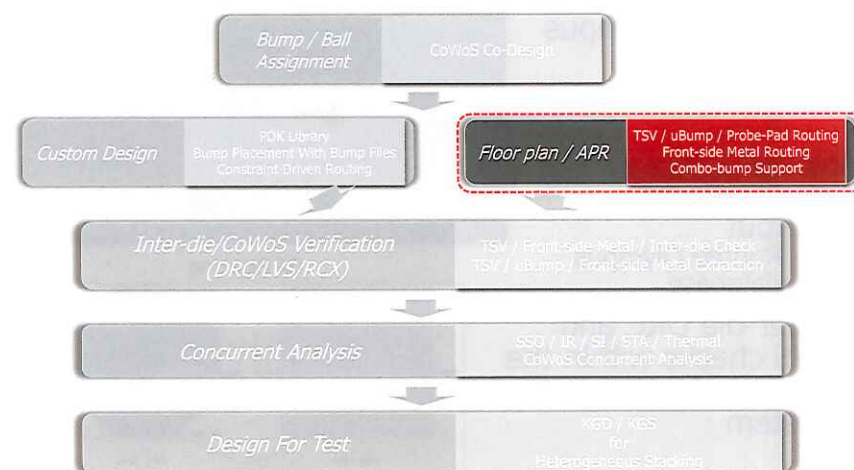
Mentor Graphics® Pyxis® Full-Custom, Routing



CoWoS Implementation

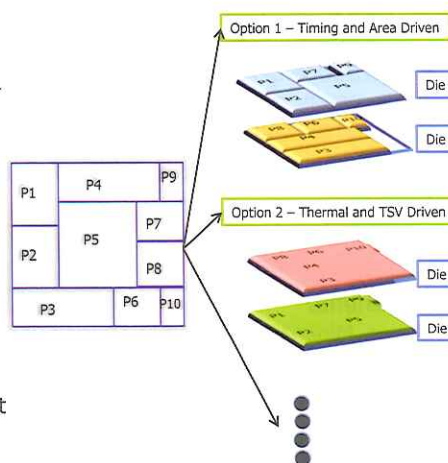


Mentor Graphics® Olympus-SoC™ Floor Plan/P&R



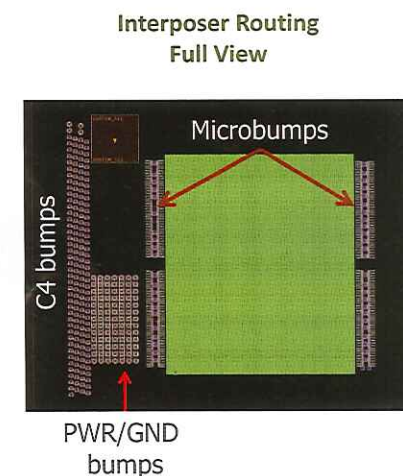
3D IC Impact on Place and Route

- Physical Implementation Considerations:
 - Floor planning → Multiple constraints drive intra- and inter-die partitions
 - CTS → Balancing complexity across dies
 - Timing Analysis → TSV characteristics and inductive effects
 - Parasitic Extraction → Impact of intra-die coupling & RLC
 - IR Drop & Thermal Analysis → Inter-die drop and thermal runaway analysis
 - Routing - 3D routing for adjacent dies



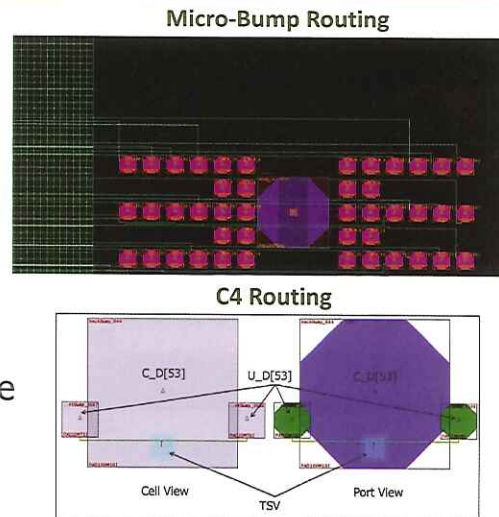
Olympus-SoC Interposer Features

- Interposer probe pad routing
- Combo-bump implementation
- Inter-die DRC/LVS check
- Bump placement considering bump spacing
- Auto-aligned block placement
- Same-signal bump group routing target
- 45 degree routing support for RDL and MB



Interposer Routing – Micro Bump and C4

- Silicon Interposer routing in Olympus
- Inputs
 - Verilog netlist
 - Bump file
 - LEF Files
 - Routed signal nets
- Output
 - Routed Olympus database
- Inter-die DRC and LVS checks within the implementation system

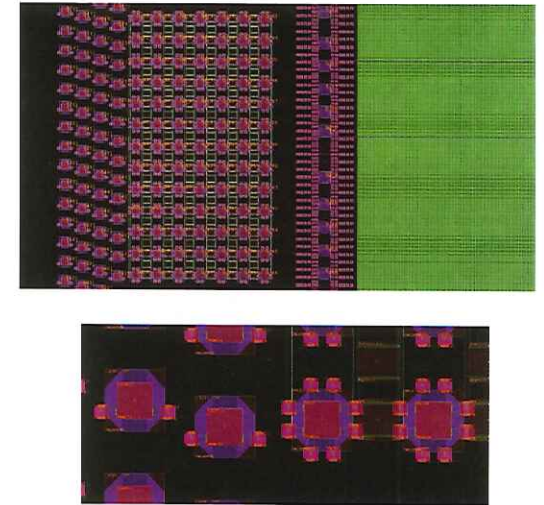


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Combo-Bumps Support

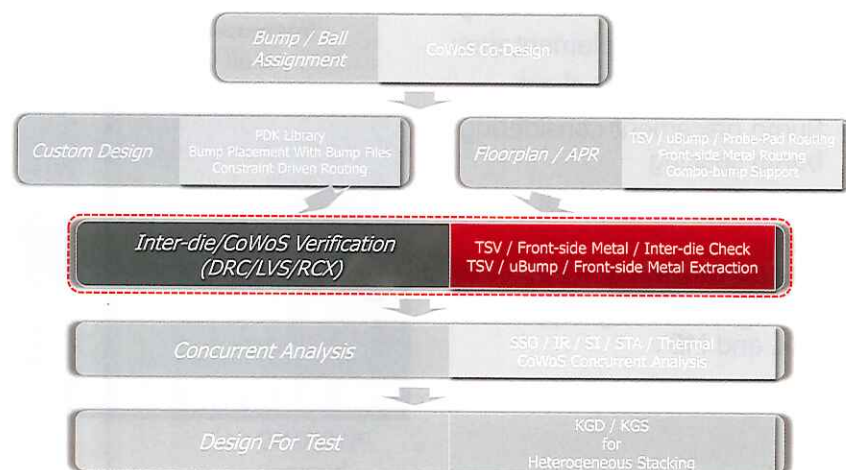
- Automatic recognition and routing between combo-bump pair based on distance
- Support for combo-bump stream-out in LEF and GDS
- Auto recognition and routing of MT-type bump including two metal layers



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Mentor Graphics® Calibre® Verification

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Calibre 3D Stack Verification Solution

- Maintain standard DRC, LVS, PEX verification processes
 - Verify independent die
- Introduce 3D interface verification solution
 - Verify physical: offset, rotation, scaling, etc.
 - Trace connectivity of interposer, or die, to die
- Good for interposer and 3D configurations, analog and digital flows



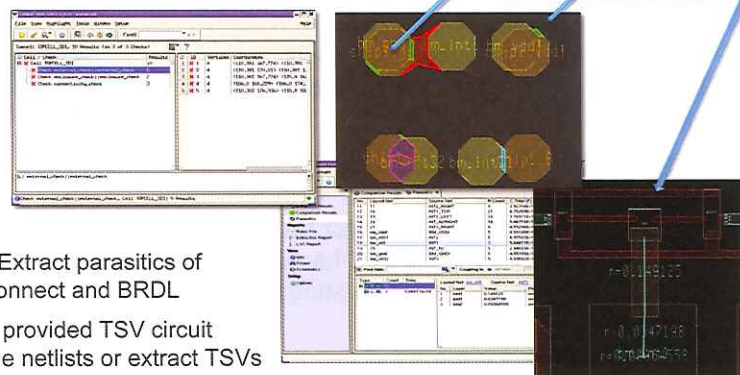
- Benefits
 - Minimal disruption to existing verification flows
 - Support flexible stacking configurations of multiple dies
 - Maximum flexibility
 - Use different process nodes and different stacking configurations (Interposer-based and full 3D)
 - Extendibility
 - to incorporate new extraction/verification solutions

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Interposer and 3D Physical Verification

- DRC: verify micro-bumps are physically aligned
- LVS: verify proper electrical connectivity through die interposer interfaces



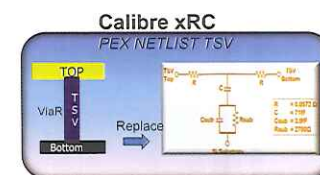
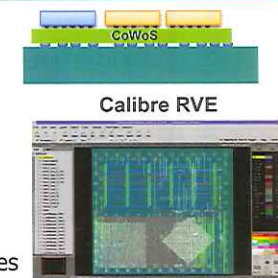
- PEX: Extract parasitics of interconnect and BRDL
- Insert provided TSV circuit into the netlists or extract TSVs and their interactions



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TSMC CoWoS Reference Flow 2012: PV

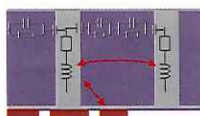
- Performs LVS/PEX on each die and CoWoS separately using Calibre nmLVS/xRC
- If LVS is clean, additional interface checking is done to ensure correctness of entire design
- Interactive debugging using Calibre RVE
- In order to run LVS on the CoWoS, bumps are identified with a PORT object but not made into nets. This allows multiple port locations with different names to coexist on the same net without causing shorts
- The port name assigned to the device so that it can be uniquely matched in the source
- Calibre xRC extracts the parasitics of the dies and CoWoS
- Calibre xRC supports insertion of provided circuit into parasitics netlist



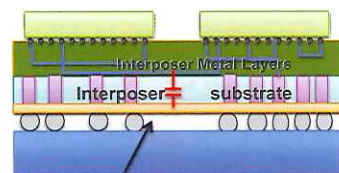
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Issues in Extracting Interposer Parasitics

- Present solution and flow good for applications with regular layout, low density TSVs.
- Not adequate for high density, high frequency applications
- Problem with non-uniform environment around the TSVs
- Does not account for TSV interactions with other TSVs, interconnect interactions between the TSV and RDL



- Interposer metal coupling might be significant (Interposer substrate is floating)
- Hard to take into account with rule-based extraction due to semiconductor substrate and frequency dependence of couplings
- Substrate treated as
 - Dielectric (for higher frequencies)
 - Floating Metal (for lower frequencies)
- Not accurate for all frequencies of interest
- Field Solver-based solution might be needed



In Interposer Configurations this coupling might need to be modeled!?



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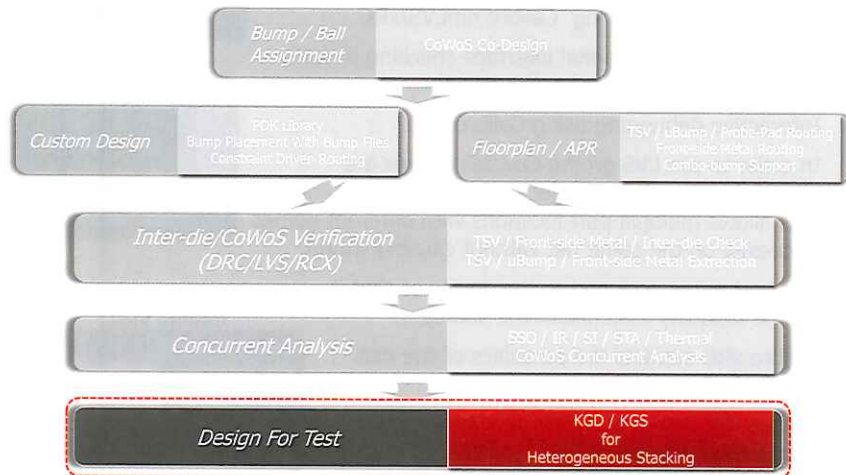
Mentor-Supported Modeling Approaches

- Single TSV models
 - Advantage
 - Easy to integrate into a flow ; Sufficient for low density TSVs
 - Challenges
 - Not adequate for high density, high frequency applications
- Compact parameterized TSV models
 - Advantage
 - Can account for some interactions; Faster than FS
 - Challenges
 - Hard to account for all situations, to parameterize for all important variables
- Field solver-based TSV extraction
 - Advantage
 - Most accurate
 - Challenges
 - Performance; Integration



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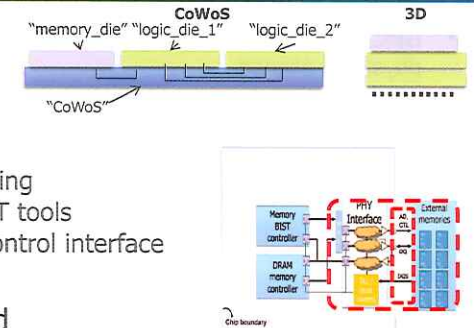
Mentor Graphics® Tessent® Test



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TSMC CoWoS Reference Flow 2012

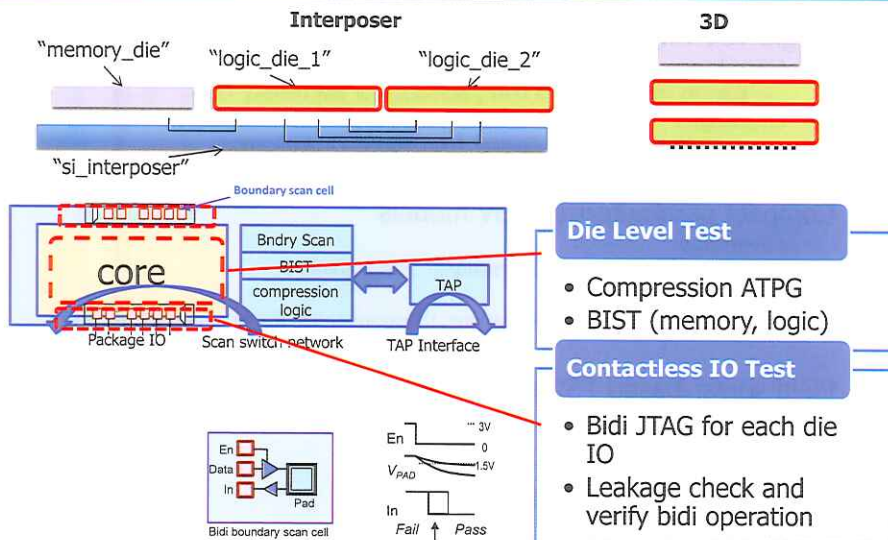
- Flow effective for
 - CoWoS
 - 3D stacked die
- Flow incorporates
 - TestKompress pattern retargeting
 - Netlist editing with Mentor DFT tools
 - IEEE P1687 (IJTAG) for test control interface
 - Memory BIST for wideIO RAM
- New test methods introduced
 - Scan switch network with RPCT
 - Logic die to logic die interconnect tests
 - Logic die to memory die JEDEC-based interconnect tests
 - Contactless IO leakage test (existing capability)



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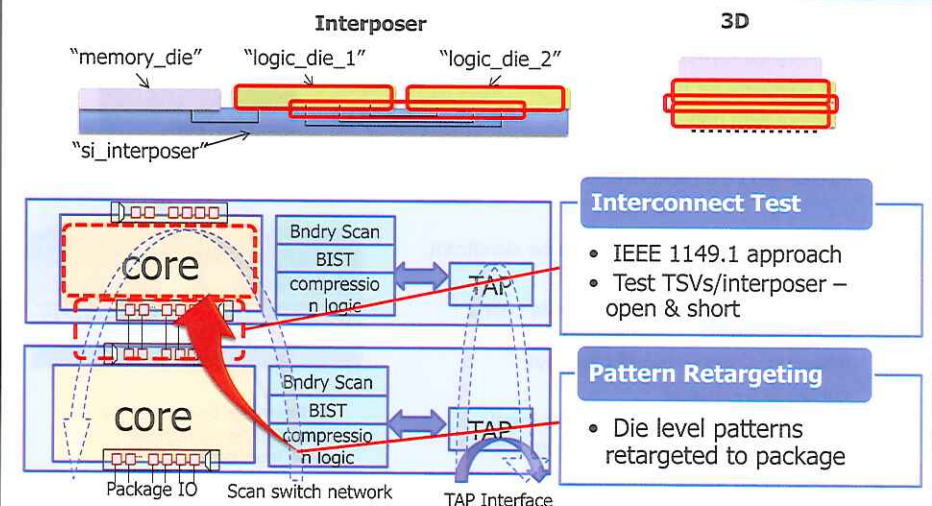
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Pre-bonding Test



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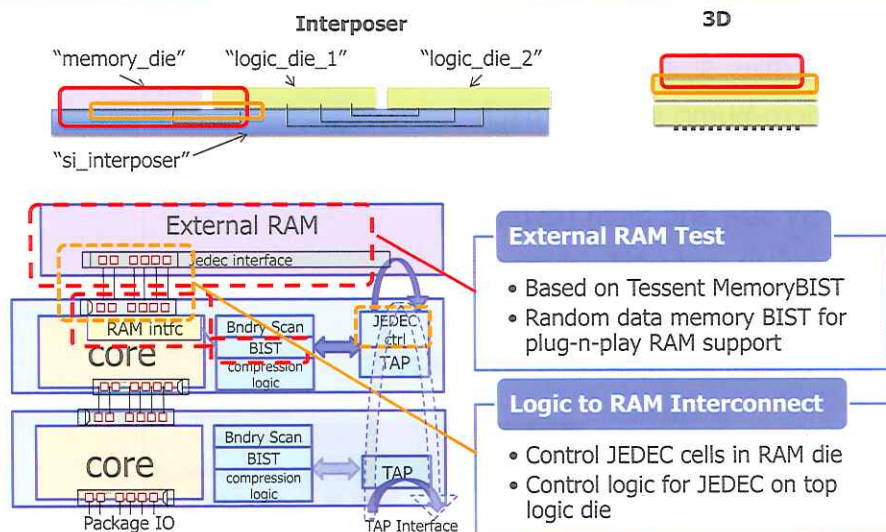
Post-bonding Test: Logic-to-Logic



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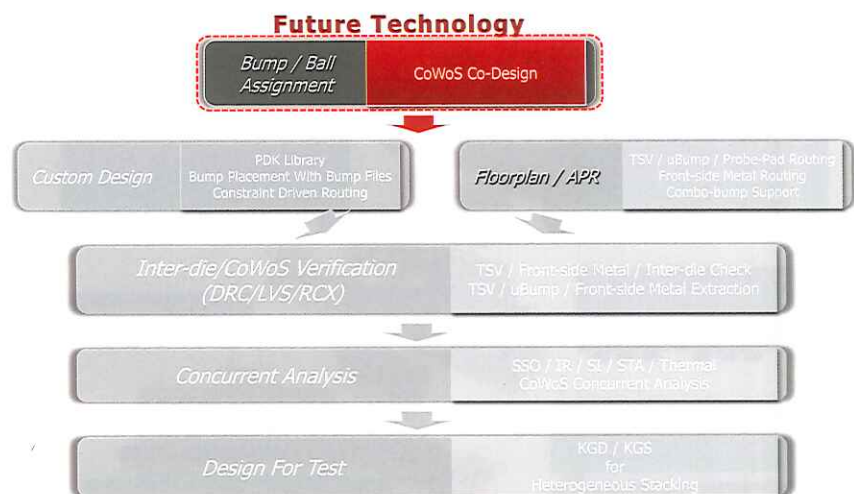
Post-bonding Test: Logic-to-RAM



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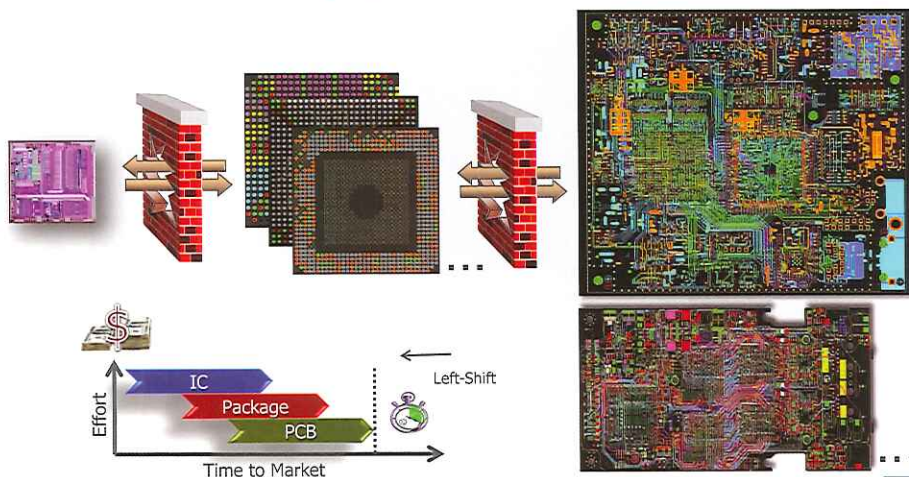
Mentor Graphics® Expedition® Package and Co-Design



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Path Finding and Co-Design for the Next Generation of 3D, IC Packaging

Evaluate multiple packaging options in the context of multiple PCBs

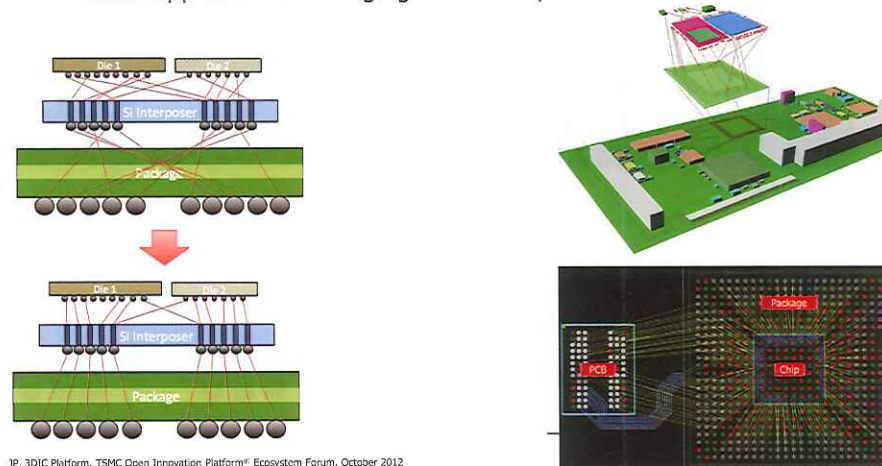


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3D Packaging; Off-Chip Connectivity...

- Complexity of the off-chip interconnect network
 - New structures to manage; TSV, micro-bumps
 - Excel approach to managing the off-chip interfaces is broken.

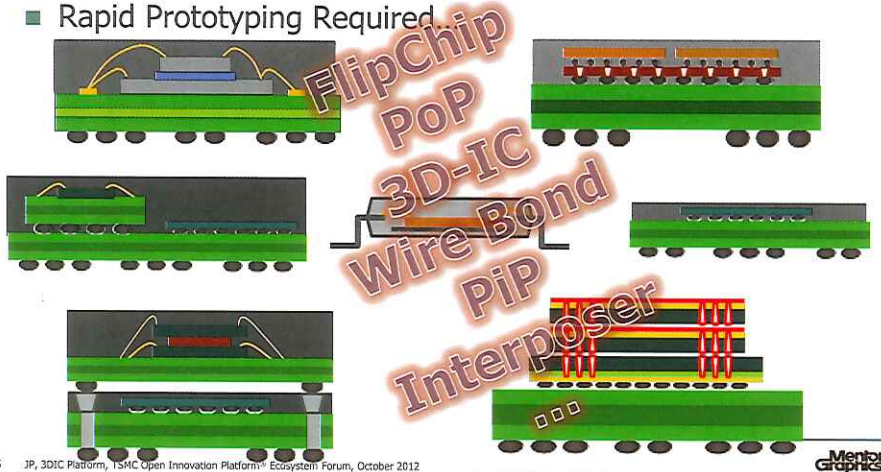


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Package Level Path Finding...

What is the "right" choice/technology for your Package?

- Cost, Size, Performance, etc.
- Rapid Prototyping Required

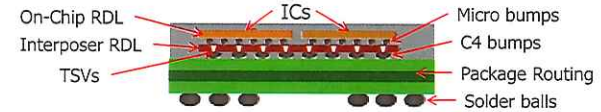


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Path-Finding Details; Interposer

- Interposer material
 - Glass, Si, etc.
- Micro-bump size and pitch
- Number of interposer metal layers
- TSV size and pitch (dynamic)
- C4 Size and pitch (dynamic)
- Package layers
- Package pin pitch and array size

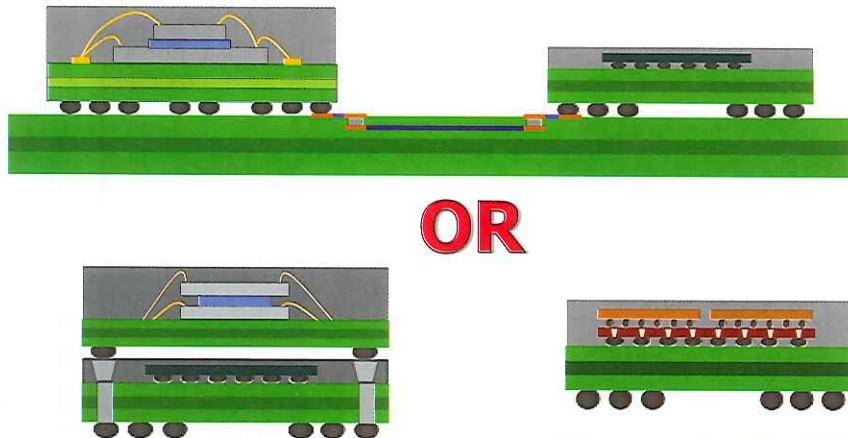


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Holistic Co-Design; PCB and Path Finding

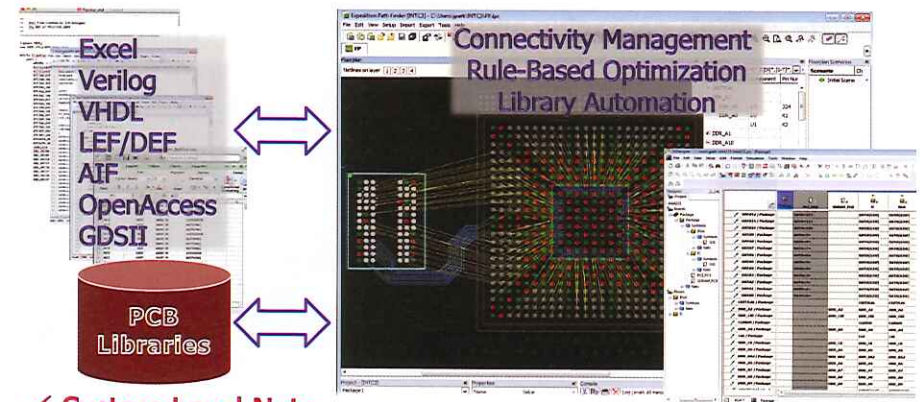
Determining the "right" solution often involves board level trade-offs...



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IC ↔ Package ↔ PCB Co-Design Cockpit



- ✓ System Level Nets
- ✓ Route Target Optimization
- ✓ Multiple Scenarios
- ✓ Board Level Interfaces (Parts)

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Summary

- Mentor Graphics provides a robust set of tools that address the challenges of CoWoS technologies
 - Advanced place & route support
 - Industry leading verification solutions
 - Industry leading test solutions
 - Co-Design across IC, Package and PCB design domains (Future)

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Thank you TSMC and Mentor Graphics contributors!

- TSMC
 - Anderson Chiu
 - Steve (Chao-Yang) Yeh
 - Donovan J.-J Chen
 - Jonathan Yuan
- Mentor Graphics
 - Sudhakar Jilla
 - Arvind Narayanan
 - Dusan Petranovic
 - Ron Press
 - Myron Lin
 - Angela Wong

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How to Manage Variability and Double Patterning at 20nm

Cadence



ABSTRACT

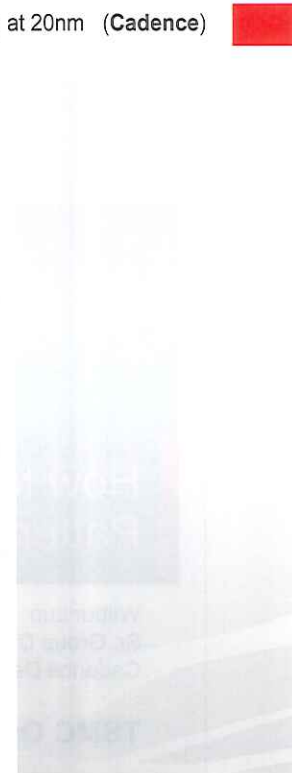
Analog and full custom design at 20nm will present a significant challenge for design engineers and layout designers. At 20nm the addition of double patterning, local interconnect, > 400 new rules, and increased variability will require a change in both design/layout methodology as well as new capabilities in EDA tools. Increased productivity and predictability and reduced over-margining will be required to recognize the maximum potential of this advanced node.

Variation is an issue increasing at every node. Layout dependent effects (LDE) can effect transistor performance by 30%. This variation must be accounted for as early in the design cycle as possible – ideally during circuit design. In addition, double-patterning can cause variation due to mask misalignment – which effects parasitics and timing.

LDE effects are a direct function of how a layout is realized – how multiple fingers of a device are interdigitated, the distance of a device from a well edge, the distance of one active region from another etc. These effects directly impact the characteristics of a transistor like mobility and threshold voltage and thus result in changes to the circuit behavior. LDE is not just a layout problem, but they are something that needs to be accounted for in the entire design flow and requires a shift in design methodology. In addition to identifying devices that are sensitive to LDE, a designer has to be able to access accurate layout effects early in the design cycle – even if with a partial placement – waiting for a DRC and LVS clean layout could cause long design iterations. Similarly, a layout engineer has to carefully place and interdigitate sensitive devices in the layout. During layout finishing, the layout engineer has to ensure that layout effects do not impact transistor characteristics drastically and needs a way to identify LDE hot spots quickly and effectively. The layout engineer will need to backannotate the LDE parameters from the LDEanalysis to the schematic and rerun the simulation. At each step in the design flow, the circuit designer needs to be able to verify the performance of the circuit in the presence of LDE without a fully DRC and LVS clean layout. Cadence and TSMC have partnered in the TSMC AMS Reference Flow 3.0 to bring a solution to market that gives mutual customers a big advantage at advanced nodes.

Managing the complexity of the 20nm and double-patterning rules requires a more intelligent, correct-by-construction, color-aware design environment. Designing in a color-aware environment will both reduce the layout time to create double-patterning clean layout and also create layout that adheres to the designer's intent. For example, analog/custom designers have requirements to match special nets/circuits. This design intent can be specified as constraints and carried throughout the flow – ultimately driving and maintaining the coloring of the nets. In the correct-by-construction environment, complex 20nm rules are adhered to and verified by using a 20nm-enabled design-rule-driven editing system and a signoff verification system integrated into the custom design platform.

Increasing productivity and predictability at 20nm requires a unified and complete approach that spans circuit design/simulation to layout implementation to verification.



How to Manage Variability and Double Patterning at 20nm

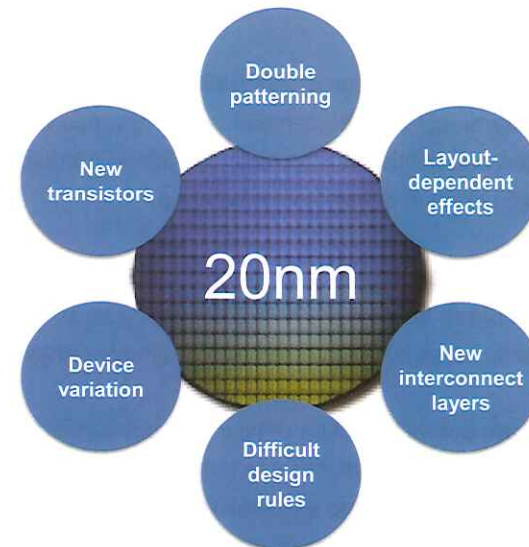
Wilbur Luo
Sr. Group Director, Product Management
Cadence Design Systems

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Challenge: Manufacturing Complexity

It's all new again compared to 28nm design



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Layout Dependent Effects at Advanced Nodes

Variation comes in all different sizes

Layout Dependent Effect		45nm	32nm	20nm and below
WPE	Well proximity effect	x	x	X
PSE	Poly spacing effect	x	X	X
LOD	Length of diffusion	x	X	X
OSE	OD to OD spacing effect	x	X	X
LPC	Layout patterning check	x	x	X
OP/PO Density	OD/poly density	x	X	X

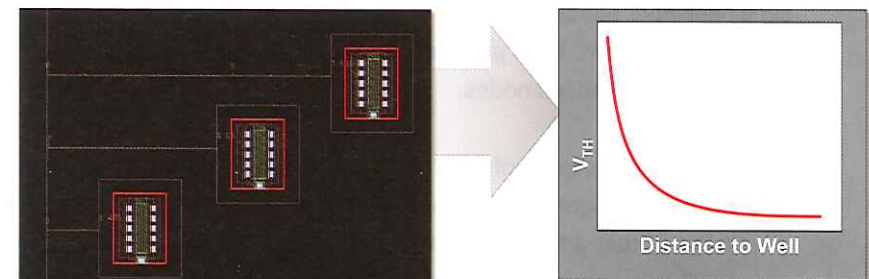
LDE is an increasingly significant form of variation at lower process nodes

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LDE Example: Well Proximity Effect

Threshold voltages can vary between 20% and 80%



• Additional physical effects:

- Shallow trench isolation (STI)
- Interconnect parasitics
- Dummy fill usage
- Lithography choices

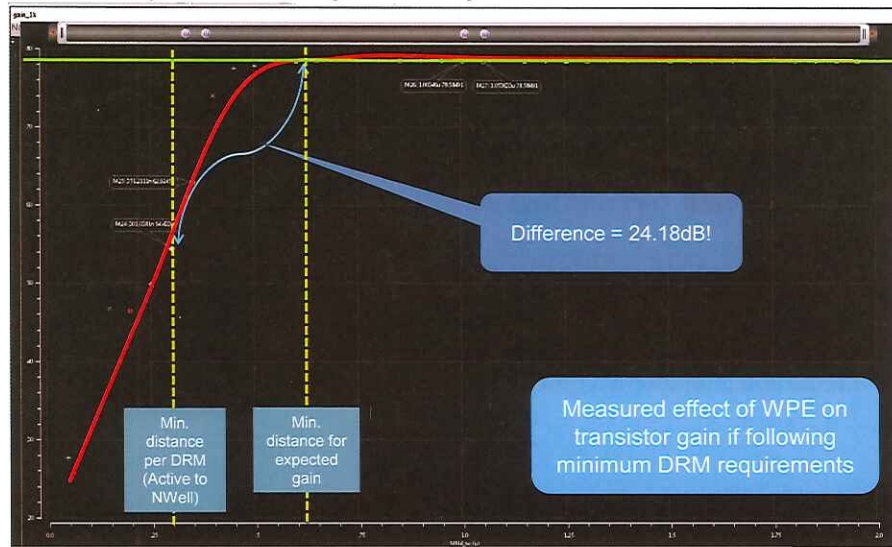
Now the layout is the design

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LDE Example: Well Proximity Effect

Transistor gain substantially affected by WPE



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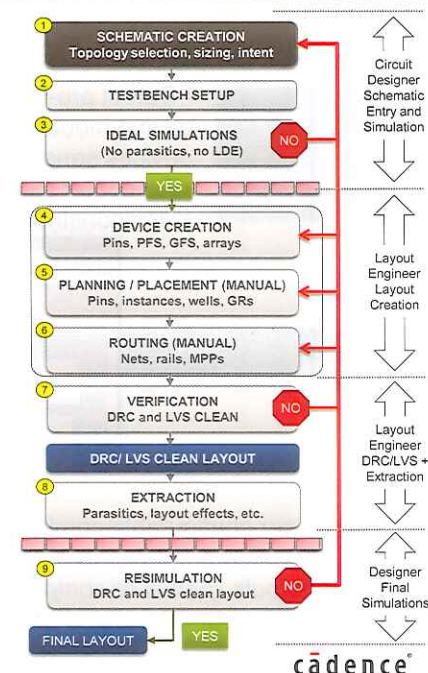
Traditional Design Flow

Limitations

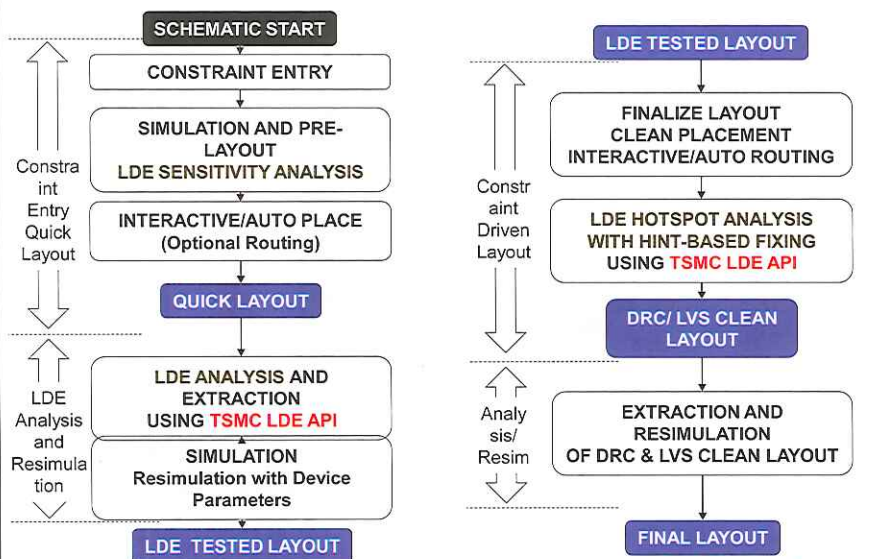
- All or nothing (no incremental analysis)
- Issues detected very late in the design process
- Physical effects not brought upfront during circuit design
- Time-consuming serialized methodology
- “Over the wall”

We need to bring layout effects early and incrementally into the flow!

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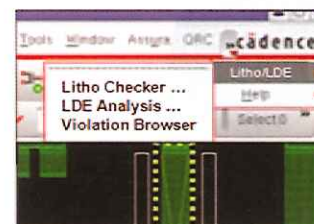
Integrated LDE-Aware Design and Analysis Flow



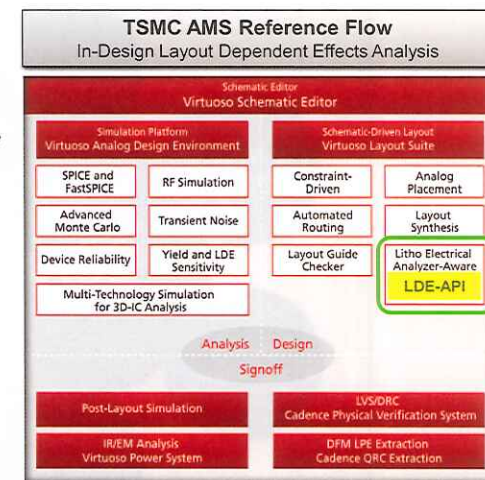
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Using Virtuoso with the TSMC LDE-API

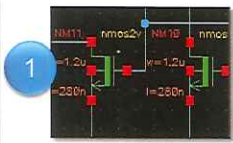
- LDE-API is available for download from TSMC
- Works with Virtuoso-DFM and LEA to identify LDE hotspots by looking at the following circuit characteristics:
 - Idsat, vth, gm, gds, vdsat



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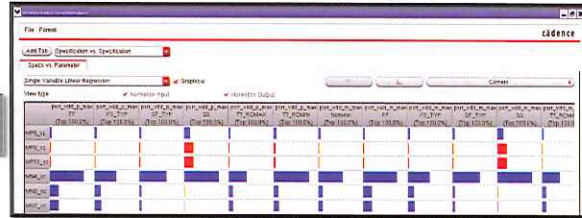


Analysis of Layout Dependent Effects in Virtuoso



- Detect pre-layout LDE sensitivity effects using the device models supplied in the PDK to quickly identify devices sensitive to layout effects.
- Re-center existing IP based on new information
- Use constraints to drive LDE aware layout

LDE Sensitivity
Analysis in ADE



Choose a user configurable combination of Pcells, MODGENS and auto-placement to quickly generate prototype layouts (*partial or complete*) to re-simulate with accurate layout effects and debug problems



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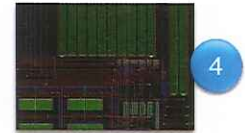
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Analysis of Layout Dependent Effects in Virtuoso



Use in-design verification to detect trouble areas during detailed layout generation. Identify LDE hotspots and use hints to fix. Verify constraints specified by circuit designer for electrical matching

Use sign-off LVS and extraction flows for final verification of circuit behavior with both layout effects and interconnect parasitics

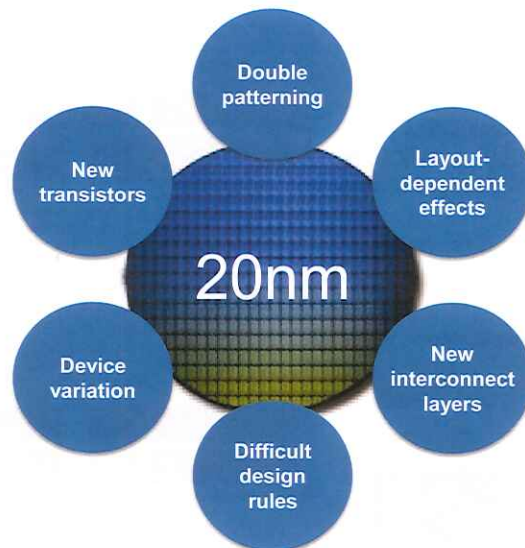


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Challenge: manufacturing complexity

It's all new again compared to 28nm design

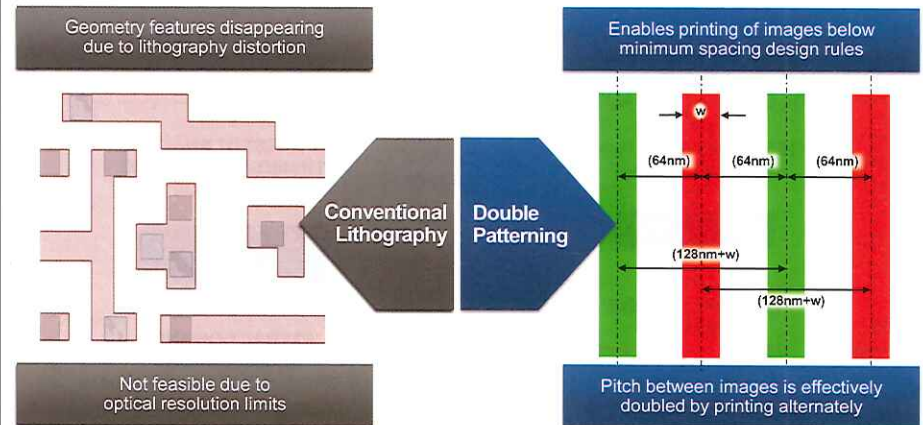


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Double Patterning Technique

A "must-have" at wire pitches smaller than 80nm



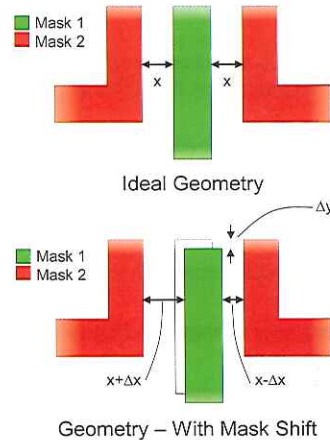
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20nm Challenges

Design complexity

- Double patterning (DPT) impacts a circuit's electrical performance
 - Different masks on a given layer will shift during the manufacturing process
- Mask shift causes variations in the polygonal data and this has a direct impact on RC on the interconnect
 - In the example to the right, coupling between net1,net2 is lower than coupling between net2,net3
 - Impacts coupling to lateral neighbors as well as fringe to layers above and below
- Makes matching a challenge!

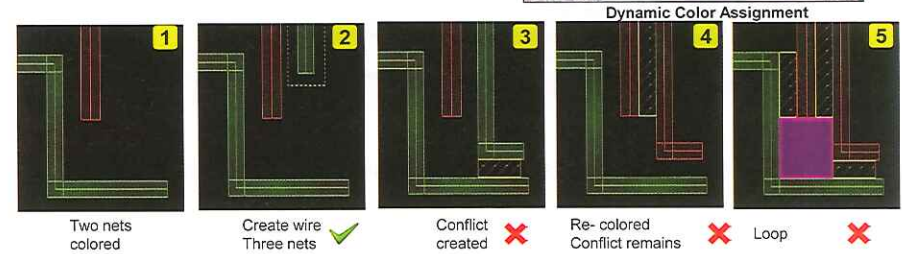
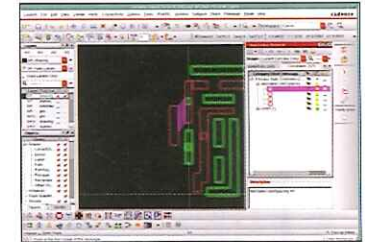


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Double Patterning Custom design – Dealing with DPT and Loops

- High priority for base IP creation to minimize area for
 - Standard Cells Library Creation, Memory, IO's, Analog Macros, etc.
- Must be cognizant of coloring while creating layout to optimize area



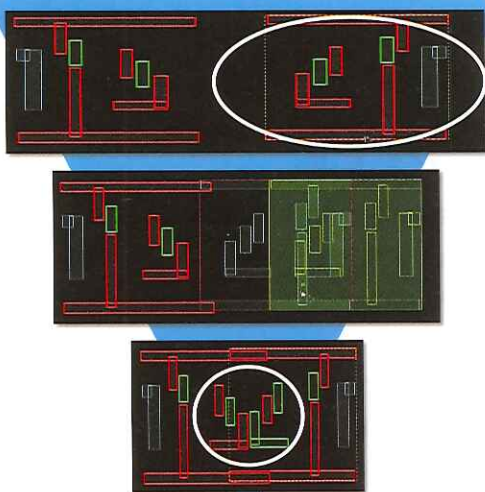
It isn't just a matter of flipping a shape
THINK about the ripple effect throughout the entire design

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Custom: Automated Color-aware Layout

Colors set as connections are made



- Cognizant of coloring to create area-optimized layout
 - Real-time colorization as layout is drawn
- As groups of shapes are moved, color will be rippled as needed throughout the shape
- Ability to lock and store colors on critical nets/geometries

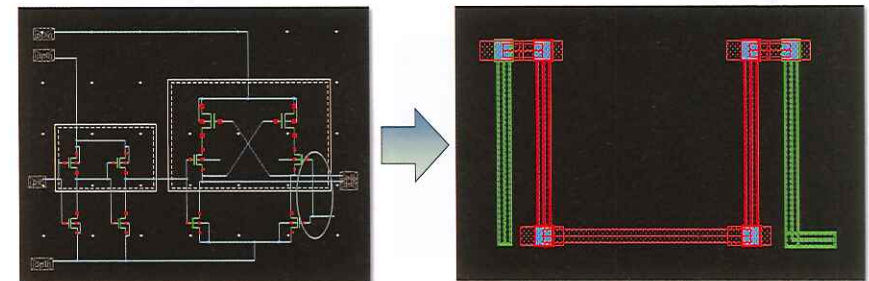
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Custom: Automated Color-aware Layout

Constraint driven pre-coloring flow

- User selects a group of one or more **critical nets** in the schematic and assigns a color constraint
 - **Matches color** on a per layer basis across all critical nets
- Cross-probing color matching groups on schematic and layout.
- Support of DRD

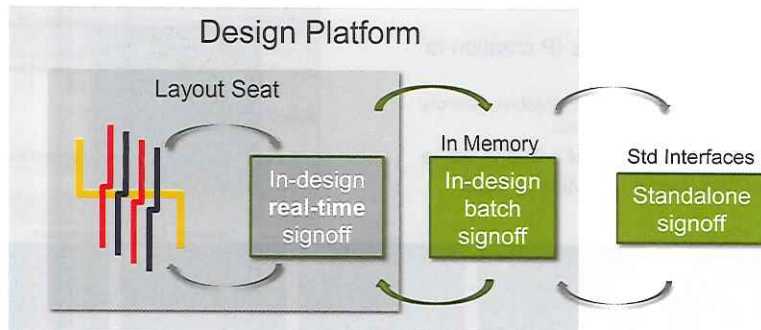


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The Key to **Speed**: “In-design” Signoff

A requirement at 20nm design



GOOD: Traditional standalone signoff using standard interfaces

BETTER: Batch in-design signoff executing off in-memory data

BEST: Dynamic in-design signoff tightly integrated into layout seat

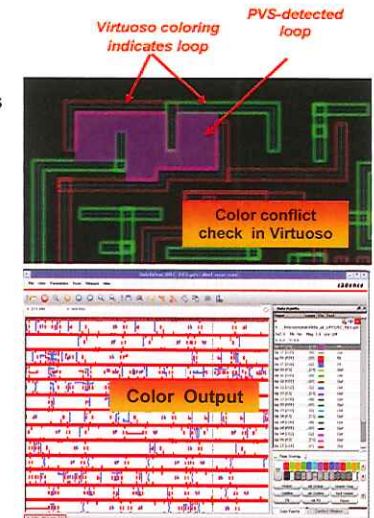
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Cadence Physical Verification System (PVS) Double Patterning Technology

Foundry and customer feedback

- “PVS DPT G0 rule check provides more accurate results and is required for all TSMC 20nm projects”
- PVS is successful in ARM Cortex-A15 tape out



- Dedicated engine approach to ensure quality and performance
- Accurate color conflict loop detection for DPT compliance check
- PVS DPT coloring decomposition results are output for more accurate device and parasitic measurements
- Integrated into the (Virtuoso® and Encounter®) design environment

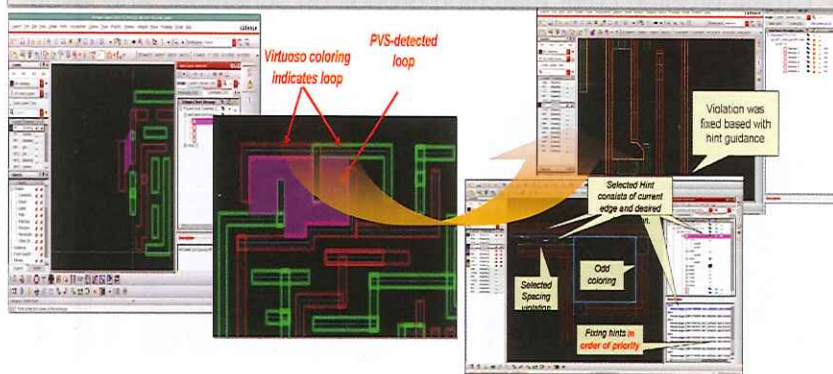
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PVS DPT in the Virtuoso Environment

Efficient in-design approach

- “Must” technology for 20nm Virtuoso in-design verification solution
- “Live” coloring loop and DRC checks based on foundry signoff deck
- Integrated with Virtuoso environment to provide unique Cadence solution from Virtuoso real-time colorization, signoff color loop detection, fixing hints to final fixing



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Virtuoso 20nm Physical Design Technologies

- Color-aware design database and constraints
- Shape-based device abutment with 20nm device support



- Local interconnect aware wire editor and router
- Color-transparent interactive use model
- Interactive Design Rule (and “odd-cycle”) Checking & hint-based fixing
- Interactive color manipulation and pre-coloring
- Interactive pattern detection for complex design rules

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Summary

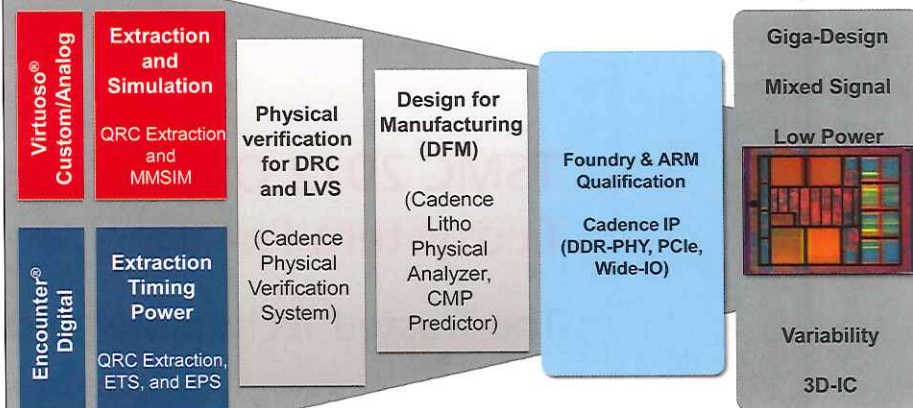
- Variation has become a critical concern and must be addressed with an integrated, front-to-back solution
- New innovations in Virtuoso address the 20nm design challenges such as DPT, local interconnect, new devices, and new rules
- Cadence and TSMC's deep and broad collaboration
 - 20nm certification
 - Custom design Reference Flow, AMS Reference Flow
 - 3D IC
 - Early test chips

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Cadence 20nm Solution

Tools + ecosystem + methodology = design success



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Award-Winning Collaboration with TSMC



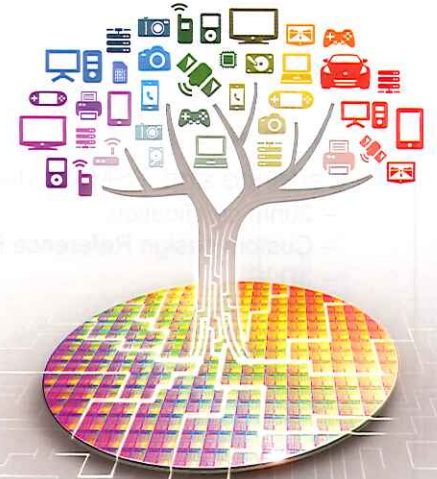
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Finding and Fixing Double Patterning Errors in 20nm Design

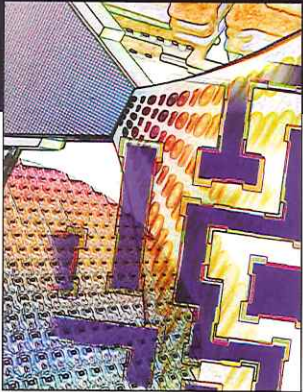
Mentor Graphics & TSMC

ABSTRACT

Double patterning brings a new set of design constraints to the 20nm node and it has caused designers to get very concerned about how they find and deal with DP related violations. In this presentation, we will explain the kinds of violations that are unique to double patterning design and how the jointly developed tools with Mentor and TSMC help identify them and aide the designer in fixing them. Examples and best practices methods will also be discussed.



Finding and Fixing Double Patterning Errors in 20nm Design



David Abercrombie

Program Manager: Advanced PV Methodology
Mentor Graphics, Design-to-Silicon Division

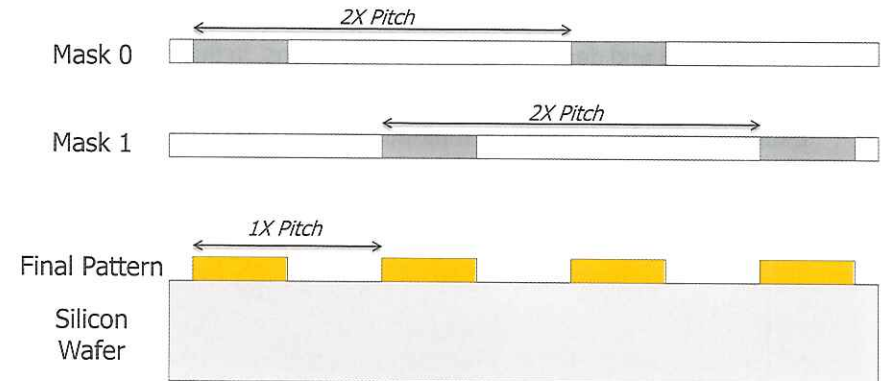
Chin-Chang (Peter) Hsu

Principal Engineer
TSMC Design Methodology Division

TSMC Open Innovation Platform® Ecosystem Forum,
October 2012



Pattern Doubling or Pitch Split (DP)



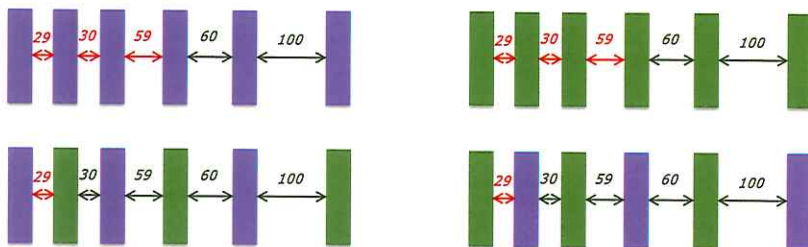
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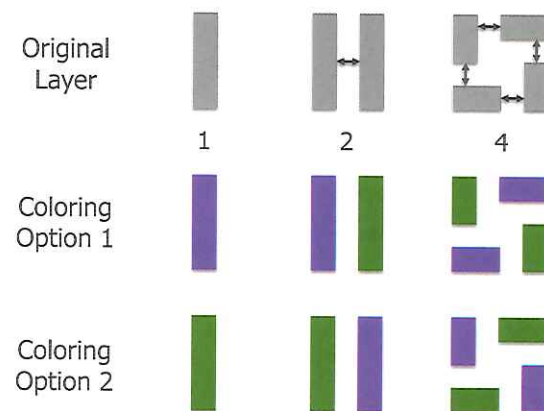
DRC Rules for DP

- Min same mask spacing (ex. $\geq 60\text{nm}$)
 - \geq "min same" can be arbitrarily colored
- Min opposite mask spacing (ex. $\geq 30\text{nm}$)
 - \geq "min opp" < "min same" Must be opposite color
 - < "min opp" not allowed regardless of color



Layer Decomposition (DP Coloring)

The act of converting a single layer into the two DP layers is called decomposition or coloring



Typically, there's more than one "correct" decomposition solution

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Rules Unique to DP

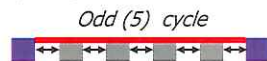
■ Odd path checks

- Odd cycle with spacing < same mask rules are forbidden



■ Anchor path checks

- Two polygons "anchored" to the same mask with an odd cycle path between them with spacing < same mask rules are forbidden

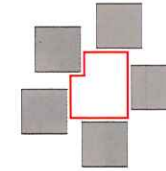


- Two polygons "anchored" to opposite mask with an even cycle path between them with spacing < same mask rules are forbidden



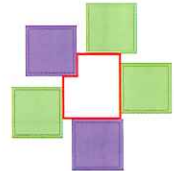
TSMC PDK DP Checks

■ DP odd path violation rule

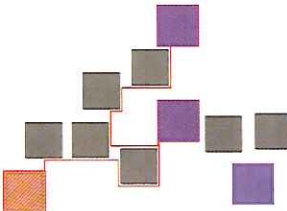


■ Mask hints

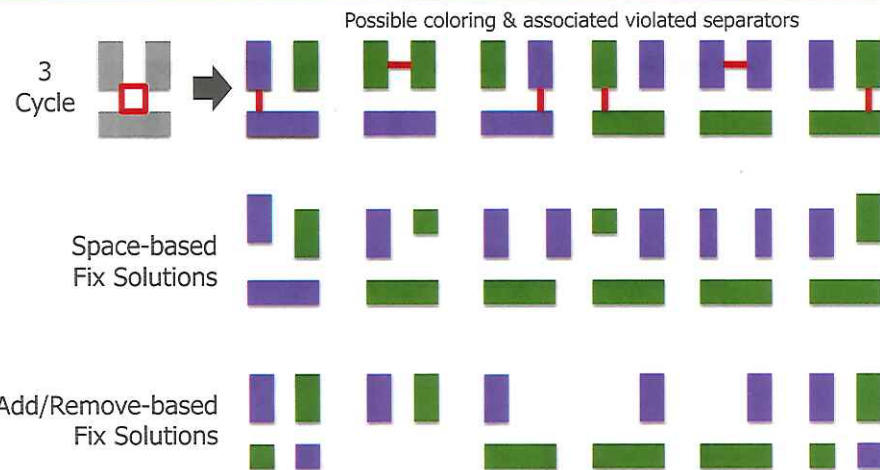
- DP colors of the odd cycle errors
- Define CALIBRE_NMDPC_MASK_HINT to activate in the deck



■ Anchor path violation rule



Fixing Odd Path Violations

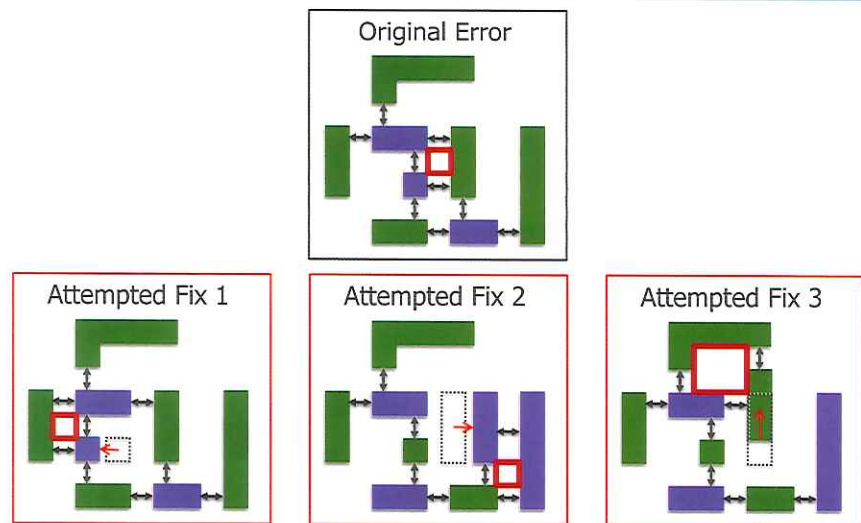


DP Debugging Frustrations

Whack-a-mole: Every time I fix a violation, another one seems to occur!



New Extrinsic Violations

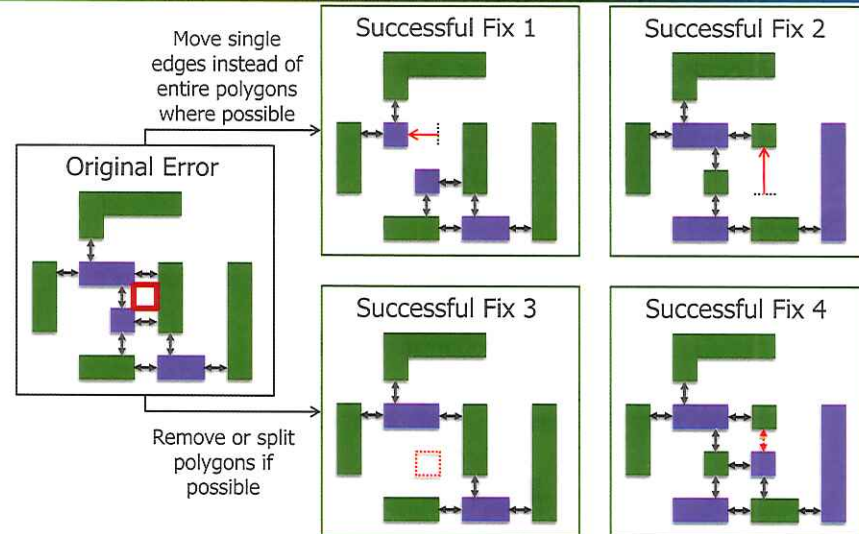


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Techniques to Avoid New Extrinsic Violations



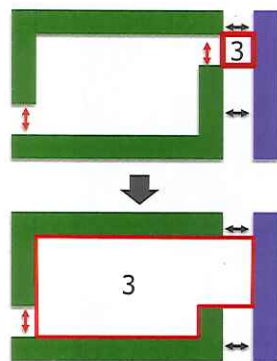
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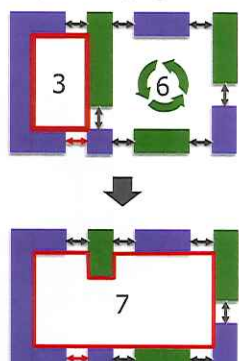
New Intrinsic Violations

Multi-Interaction Polygons



Fixing a single separator may not break the odd cycle

Cycle Propagation



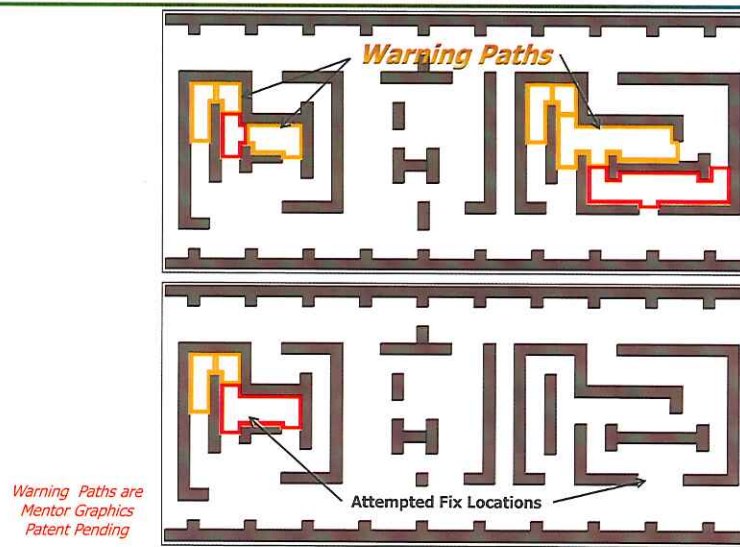
Fixing one odd cycle can lead to another odd cycle

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Debug Hints to Avoid New Intrinsic Violations

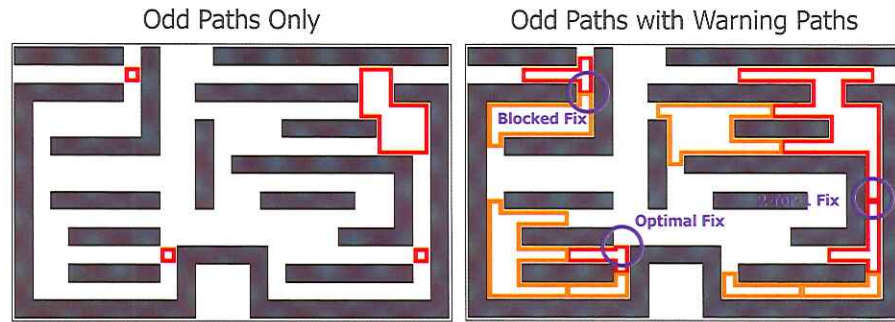


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Example Debug Options



Warning Paths are Mentor Graphics Patent Pending

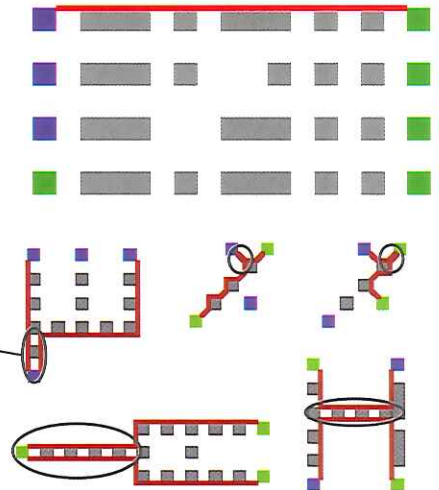
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Fixing Anchor Path Violations

- Fixing an anchor path violation is very similar to fixing an odd path violation
 - Increase any one of the spaces along the path
 - Remove any polygon along the path
 - Remove or change one of the anchors
- Separators that are shared by two anchor paths will fix both paths



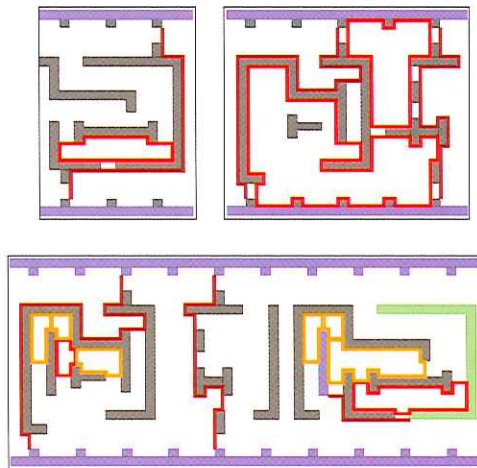
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Fixing Multiple Error Types

- It is best to first fix all the odd cycle violations before fixing the anchor path violations
- Highlight all the warning and anchor paths, and then step through each odd path violation to get the most information to help with debug



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Calibre Multi-Patterning is Part of Mentor's Comprehensive Multi-Patterning Solution

Design Implementation	Design Verification	Manufacturing
Calibre RealTime <ul style="list-style-type: none"> • Real-time MP checking and debug for custom design 	Calibre Multi-Patterning <ul style="list-style-type: none"> • MP Checking & Debug • Auto-Decomposition 	Calibre nmDP <ul style="list-style-type: none"> • Mask Decomp. & Stitching • Streamlined DP/OPC flow
Olympus-SoC <ul style="list-style-type: none"> • MP Place and Route • Auto MP violation correction 	Calibre LFD & YieldEnhancer <ul style="list-style-type: none"> • MP litho contour generation • Overlay shift verification • Colored Smart Fill Generation 	Calibre mpOPC <ul style="list-style-type: none"> • Concurrent OPC correction of both masks • Inter-layer bridge checks & model-based stitching
Calibre InRoute <ul style="list-style-type: none"> • Sign-off quality MP PV integrated into Olympus-SoC 	Calibre LVS/xACT <ul style="list-style-type: none"> • MP-Aware PEX • Multiple flow support 	Calibre OPCverify <ul style="list-style-type: none"> • MP Mask Verification

Mentor & TSMC, Working Together to Enable 20nm Double Patterning Design

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Enabling 20nm Custom Design in Laker Springsoft



ABSTRACT

In this presentation SpringSoft will show how Laker addresses the 20nm custom design challenges described in the TSMC Custom Design and AMS Reference Flow 2012. The Laker Custom IC Design platform demonstrates a commitment to the TSMC Open Innovation Platform with an open, interoperable custom design system built on the OpenAccess (OA) database that enables integration with TSMC APIs, and third-party EDA vendors to provide a comprehensive 20nm infrastructure.

SpringSoft and TSMC collaborated on several effective solutions for 20nm custom design challenges such as:

- LDE-aware analog placement automation
- Local interconnect layer support
- Real-time DPT rule checking during layout creation
- DPT pre-coloring
- Gradient density check dummy patterning insertion for HKMG analog layout
- Voltage-Dependent Design Rule Checking (VDRC)





Enabling 20nm Custom Design in Laker

Dave Reed
Sr. Product Marketing Director



Open Innovation Platform®

Laker Use for 20nm

- Multiple 20nm test chips created with Laker Test Chip Designer product
- 20nm SRAM tapeout for Laker layout editor
- Standard cell development at TSMC

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20nm Basic Layout Editing

- Foundry Support
 - TSMC Laker technology file with MCell devices
 - TSMC iPDK with TCL callbacks (v1.0 and above)
- Features
 - MCell device handles local interconnect and cut poly layers
 - Added local interconnect layers to path command

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20nm Advanced Features

- Available now
 - LDE-aware analog placement automation
 - Stick Diagram Creator handles dummy gate insertion, abutment rules, and cut-poly insertion
 - Connectivity tracing through local interconnect for schematic-driven layout and path tracing command
 - Double-patterning checks with built-in DRC checker (including pre-coloring support)
 - Also double-patterning checking with Calibre® RealTime
- Available Q4
 - Features for TSMC 2012 Custom Design Reference Flow

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Laker Stick Diagram Creator

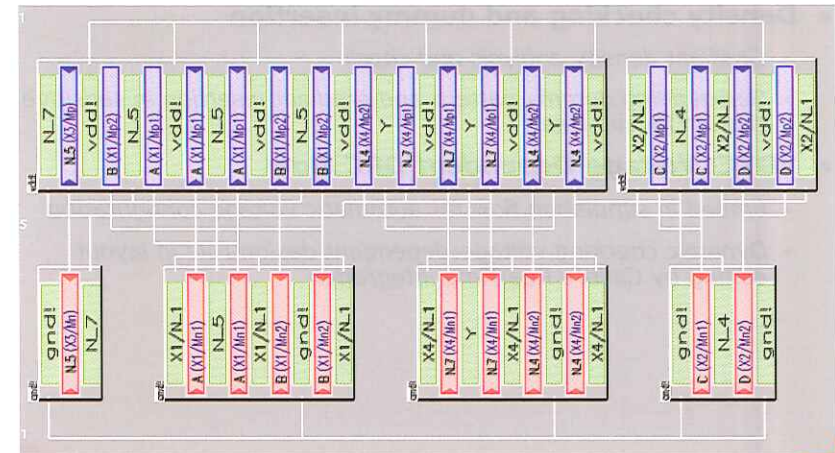
Symbolic transistor chaining

- *Symbolic manipulation is perfect for highly structured 20nm layout*
- *Users can align, swap, split and merge transistors and add dummies with simple commands*

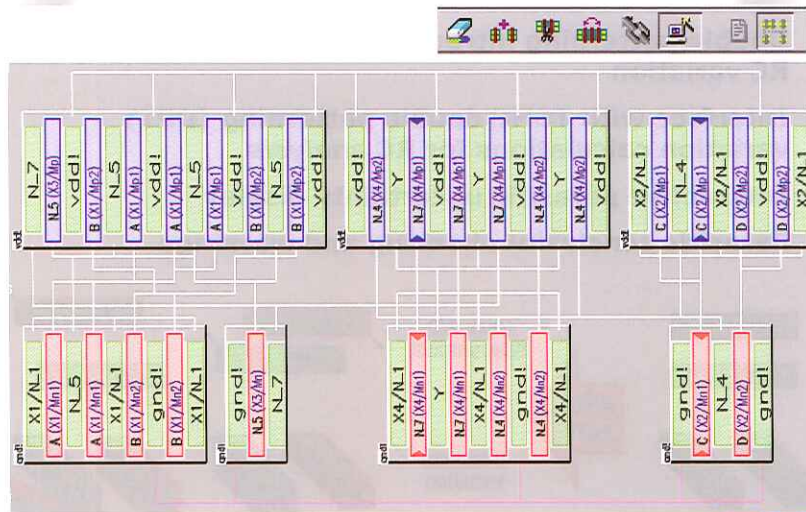
- Automatic layout generation

- Symbolic layout converted into DRC-correct 20nm layout
- Handles gate alignment, cut-poly insertion, LI layer creation, contacts to power rails, etc.

Laker Stick Diagram Creator



Same Design After User Manipulation



Custom Design Reference Flow in Laker

Design Flow for Double Patterning

- Double-patterning design rule checking in layout
- Pre-coloring
- Real-time parasitic uncertainty Δ RC analysis and constraint checking

- **LDE-aware design flow for layout dependent effects**

- Geometrical to electrical impact calculation
- On-the-fly electrical impact analysis

- **Parasitic emulation before post-layout simulation**

- Fast RC emulation for 28 to 20nm custom design porting
- RC constraint checking

Custom Design Reference Flow in Laker

- **Density checking and dummy insertion**
 - Gradient density analysis and check
 - Surrounding dummy pattern and gradient insertion in sensitive custom layout area
- **VDRC: Voltage-Dependent DRC Flow**
 - Embed in simulation flow for automatic voltage configuration
 - Dynamic checking voltage-dependant design rule in layout editing by Calibre RealTime integration

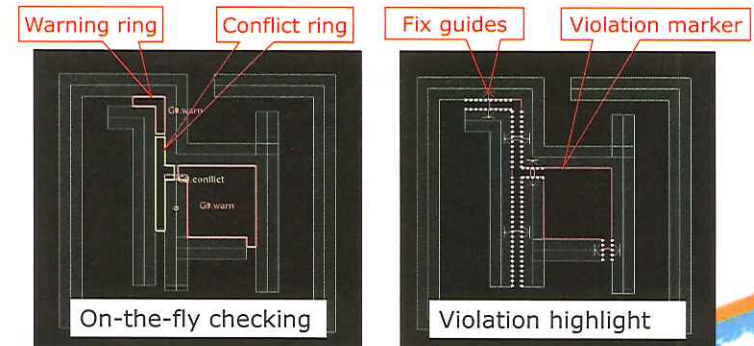
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Double-Patterning Rule Check in Layout

- **Support On-the-fly DP checking**
 - On-the-fly DRC checking and violation highlight in layout editing
 - Show fixing guide if DRC violation
 - Support pre-colored objects



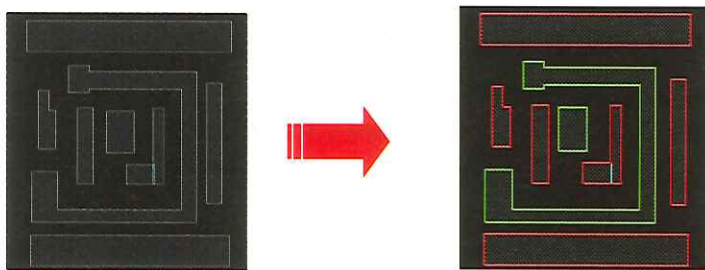
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Pre-Coloring

- **Pre-coloring engine emulates layout decomposition for double-patterning**
- **Use anchor to assign specific shapes/nets to specific mask to minimize RC mismatch**



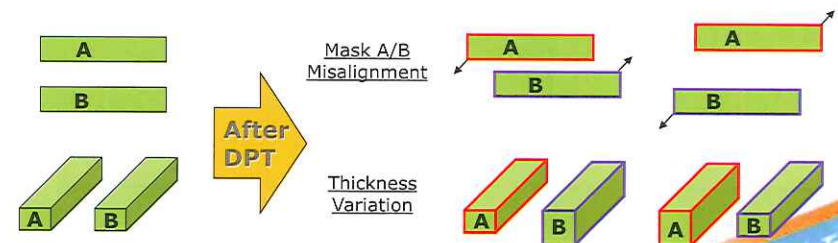
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Parasitic Uncertainty (Δ RC) Analysis

- **Double patterning introduces extra uncertainty for RC variation**
- **Interface with TSMC double patterning (DPT) variation calculations for RC analysis**
- **Interactive parasitic uncertainty display**
- **Parasitic constraint checking and warnings**

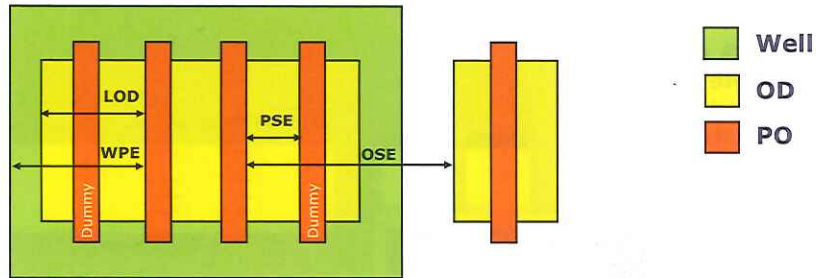


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Layout Dependent Effects



LDE impacts stress and dopant profiles...

- Stress – LOD, PSE, OSE
- Dopant profile – WPE

...that impact transistor characteristics

- V_t , I_{dsat} , G_m , G_{ds} , I_{dlin} , V_{dsat}

...that impact your circuit behavior

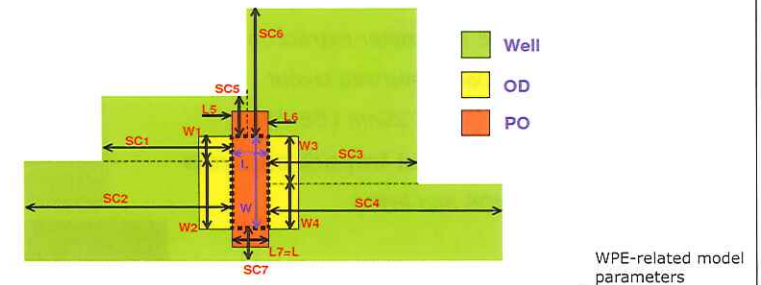
- Voltage gain, gain bandwidth, slew rate, etc.

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These Effects are Modeled in SPICE

Example: Well Proximity Effect



$$V_{th0} = V_{th0_{org}} + K_{VTH0WE} \cdot (SCA + WEB \cdot SCB + WEC \cdot SCC)$$

$$K_2 = K_{2_{org}} + K_{2WE} \cdot (SCA + WEB \cdot SCB + WEC \cdot SCC)$$

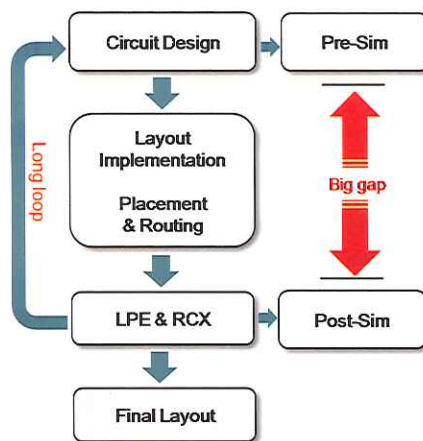
$$\mu_{eff} = \mu_{eff_{org}} \cdot (1 + K_{U0WE} \cdot (SCA + WEB \cdot SCB + WEC \cdot SCC))$$

Source: UC Berkeley BSIM4.5.0 Manual

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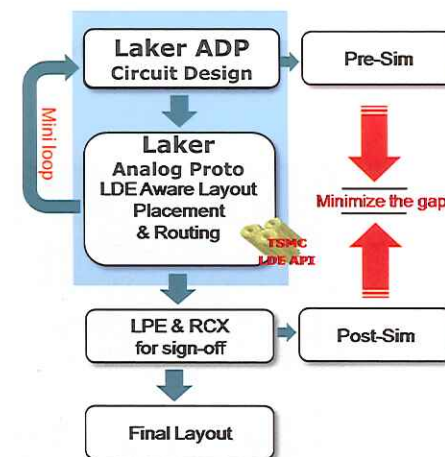
Post-Layout SPICE is Too Late



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Solution: Laker + TSMC LDE API



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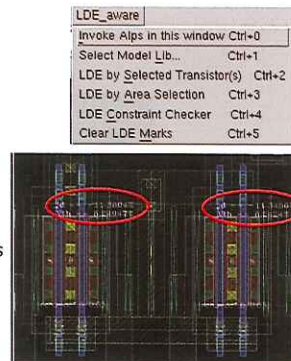
LDE-Aware Layout

Geometrical to electrical impact calculation

- Automatic LDE parameter extraction w/o LPE tools
- Support non-parameterized layout
- Integrate with TSMC 20nm LDE-API

On-the-fly electrical impact analysis

- Supports NMOS and PMOS
- Multi-finger
- Abutted device
- Multiple segment weighting for LDE parameters
- Single instance & area selection
- Show device performance degradation in % on Layout

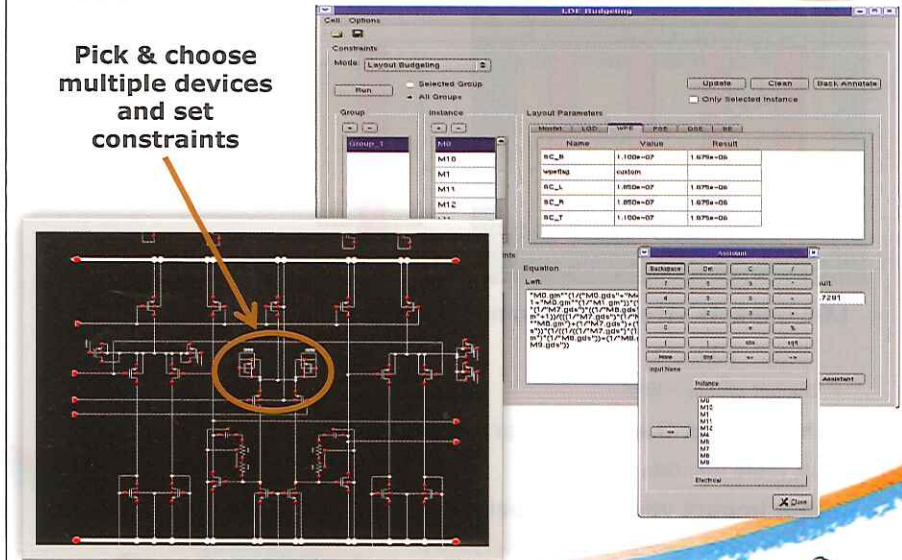


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Constraint Setup in Laker

Pick & choose multiple devices and set constraints

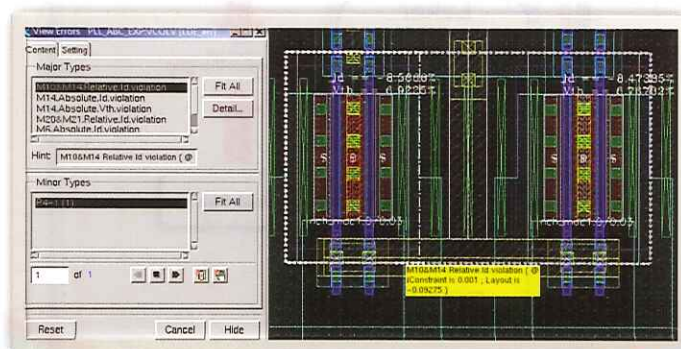


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LDE Constraint Checker in Laker

- Traverse constraint violations in error viewer
- Cross probe between errors and layout

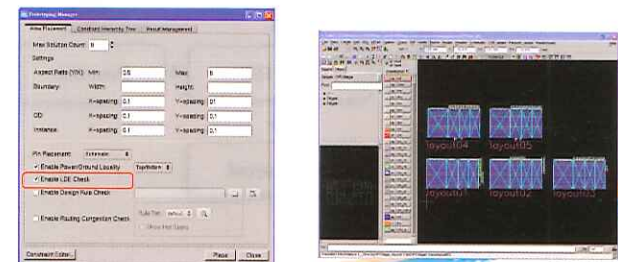


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LDE-Aware Placement

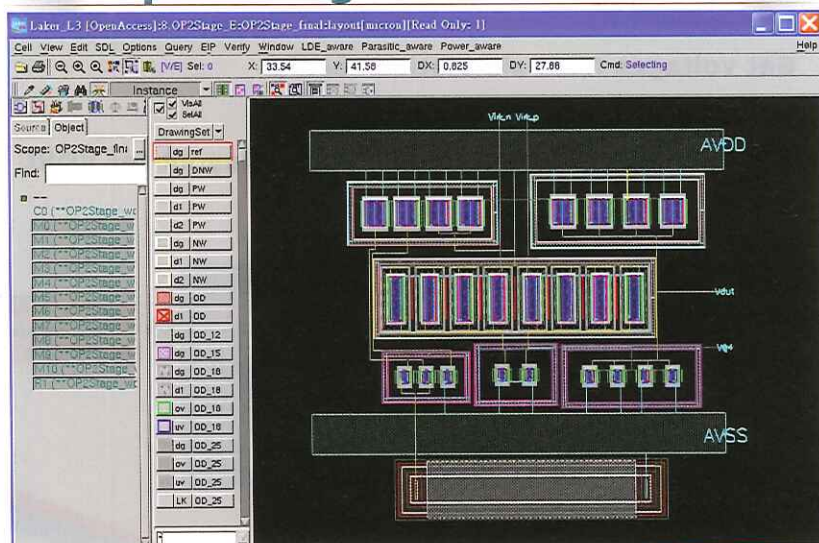
- Integrate with TSMC 20nm LDE-API
- Honor LDE budgeting result for initial placement
- Automatically check LDE constraint and fix violations
- Provides multiple solutions



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Example Design



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Example Design Results

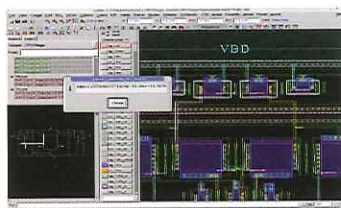
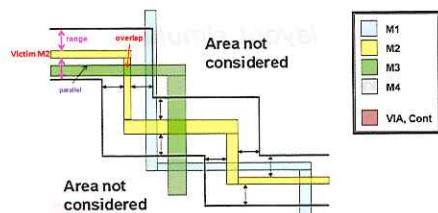
	DC gain of 2-Stage OP Amp.		Pre-Sim/Post-Sim Gap
Traditional Flow	Pre-Sim	1600.6844	17%
	Post-Sim	1366.9207	
LDE Aware Flow	Pre-Sim	1360.6311	< 1%
	Post-Sim	1366.9207	

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Parasitic-Aware Layout

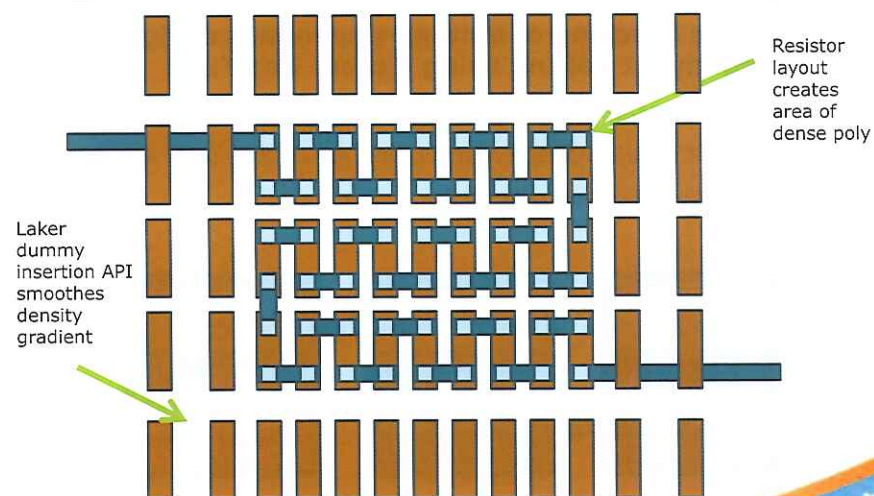
- Real-time parasitic RC analysis for layout adjustment
- Support Level-1 and Level-2 RC analysis
 - Level-1: integrate with TSMC RC calculation scripts
 - Level-2: integrate with Calibre xAct 3D solver
- Support predefined simulation corner
- Analyze RC by selected net



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Issue: Density Gradient



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Gradient Density Analysis and Insertion

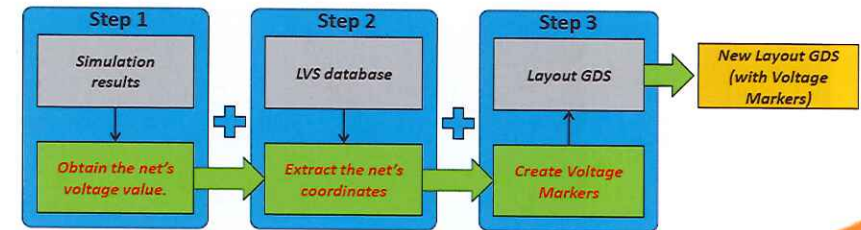
- Density calculation for specific layer
- Density map
 - Highlight density variation areas
- Dummy insertion feature

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Voltage-Dependent Design Rule Checking

- Get voltages from simulation results
- Extract net coordinates from LVS
- Create voltage marker/text layers in layout for VDRC

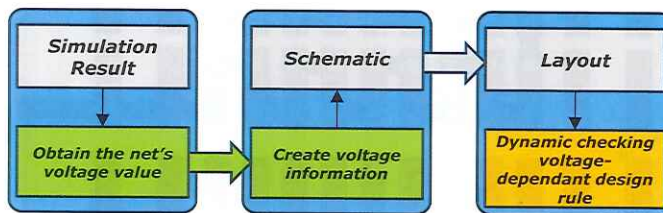


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VDRC with Calibre RealTime

- Dynamic checking of voltage-dependant design rules during layout editing using Calibre RealTime
 - Dynamic search net voltage information in OA database.
 - Dynamic create voltage marker/text for Calibre DRC engine.
 - Use Calibre sign-off rule deck.



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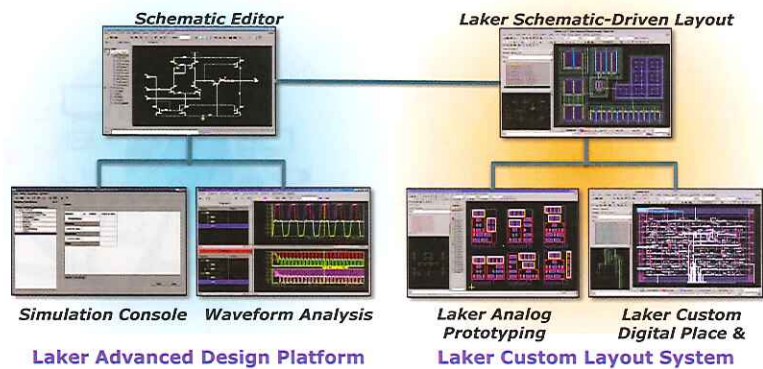
Laker is Ready for 20nm Design

- Already in use by leading customers
- Support for new Custom Design Reference Flow requirements
 - Design flow for double patterning
 - LDE-aware design flow
 - Density checking and dummy insertion
 - Parasitic emulation before post layout simulation
 - Voltage-dependent DRC flow

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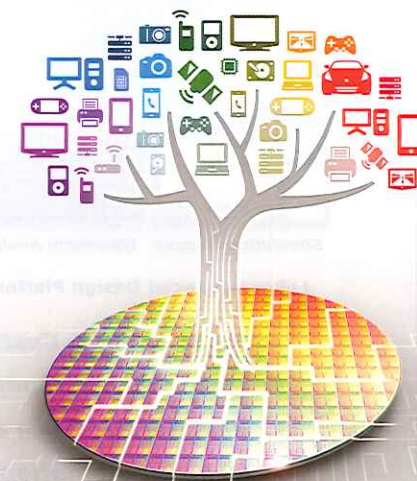
Laker³ Custom IC Solutions



- ◊ **Front-to-Back Custom Design solution**
- ◊ **Open and interoperable platform**
- ◊ **Best performance and capacity**
- ◊ **Unique automation**

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3D-IC Silicon Interposer IC Design Flow Using Cadence Encounter Digital Implementation (EDI) System

Cadence



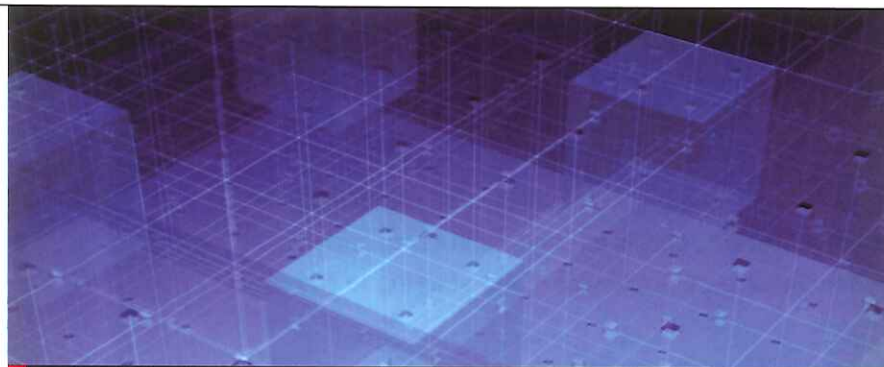
ABSTRACT

3D-IC is an alternative technology to traditional 2D circuit which reduces the pressure from Moore Law's scaling. This technology enables designers to build three dimensional integrated circuits with a great number of significant benefits realized, such as increasing interconnect bandwidth and decreasing latencies. Silicon Interposer technology reduces the complexity of 3D-IC stacking to two levels which also requires the design automation tools to support it.

As a pioneer of 3D-IC design in EDA industry, Cadence has demonstrated a solution to support 3D-IC design from implementation, analysis to verification, with the largest set of 3D-IC tape-outs. As a leading edge physical implementation, EDI has developed design flows to support both multiple stacked dies and silicon interposer design. EDI Design flow provides automation to support multiple die stacking, automation of micro-bumps (or copper pillar) and TSV, and the use of floorplanning, placement and routing to completed physical implementation. In addition, EDI provides the support of special RC extraction tuned for silicon interposer to drive sign-off analysis such as EPS (Encounter Power System) and ETS (Encounter Timing System)

Cadence and TSMC have collaborated to provide specific 3D-IC technology support in both design implementation and also sign-off analysis. In addition, we have collaborated on design methodology to support hierarchical design flow with embedded bumps (and also micro-bump) and optimization to improve routability and reduce the impact of parasitics the full 3D-IC stack. This paper introduces 3D-IC silicon Interposer physical design flow using Encounter. We will emphasize hierarchical design flow and in particular the use of TSMC combo-bump and embedded bump approach. The main emphasis is to help the user to automate such a methodology using TSMC silicon technology and optimize the results for best timing and power.





3D IC Silicon Interposer IC design flow using Cadence Encounter Digital Implementation (EDI) System

Tao Chen, Sr. Product Engineer
TSMC OIP

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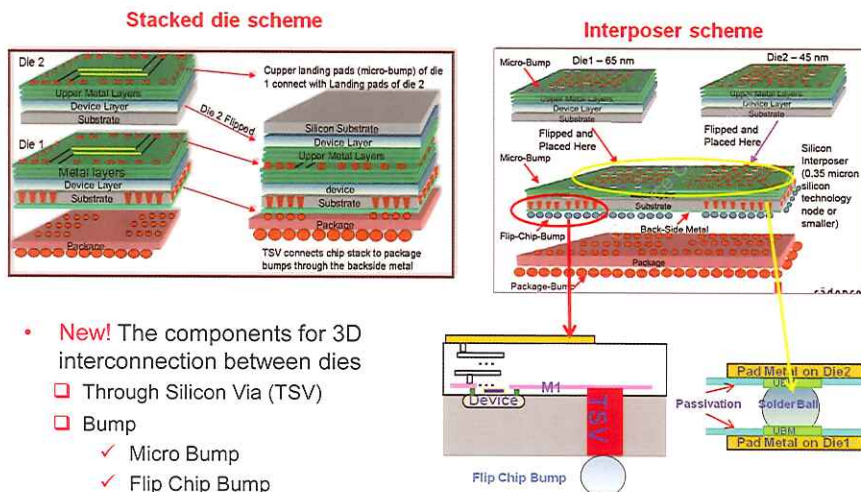
Outline

- 3D IC design tools from Cadence
- Physical implementation through EDI System
- New technology implementation through EDI System
 - Combo bump support
 - Embedded bump support
- Verification and signoff flow
- Conclusion

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What is 3D IC?



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Collaborations on CoWoS™

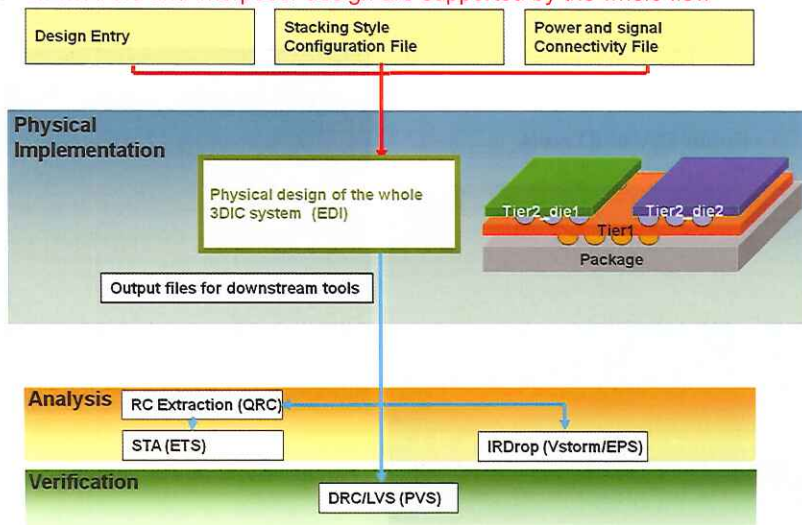
- Cadence and TSMC have collaborated to provide specific technology support for both physical implementation and sign-off analysis.
- In physical implementation, EDI supports the entire CoWoS design flow
 - Create and route TSV/bump automatically
 - Align TSV/Bump between chips automatically
- Collaborate with TSMC on design methodology to support new technology in CoWoS
 - Develop combo bump design flow supports the use of combo bump in CoWoS design
 - Develop a hierarchical design flow with embedded bumps to support large scale CoWoS design
 - This design methodology helps automate physical implementation with the new technology and optimizes the results to achieve “best” timing and power

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3D IC flow high-level description

Both stacked die and interposer design are supported by the whole flow

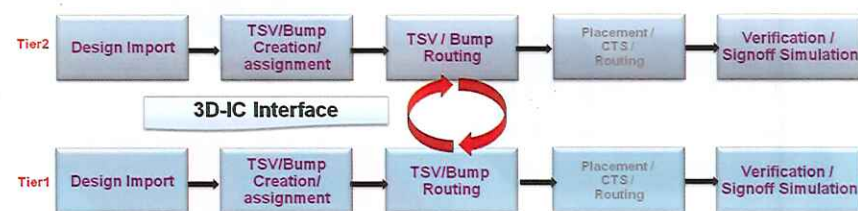


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Design flow

- EDI System is enhanced to handle TSV/bump
 - TSV is modeled as a via or cell
 - The distance between TSV and other cells could be controlled automatically
 - Bump is modeled as a bump macro
 - Support the creation of bump on both front side and back side of chip
- Optimize the design result of the whole 3D IC system
 - The nets with the same signal are aligned between all chips
 - Minimize the wire length for die to die interconnection
 - The 3D IC Interface between chips could sync up automatically or through manual work

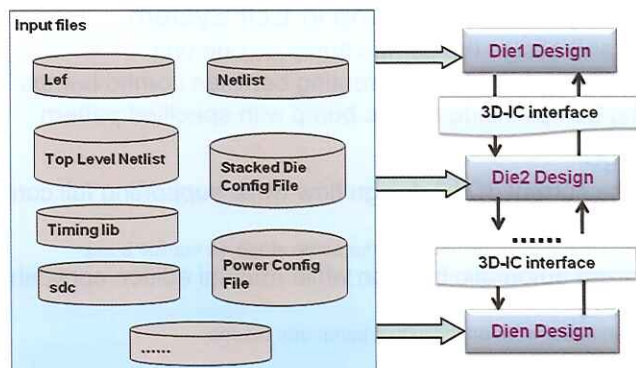


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Design import

- Define TSV/bump in LEF file
- EDI takes additional files to define connectivity between chips

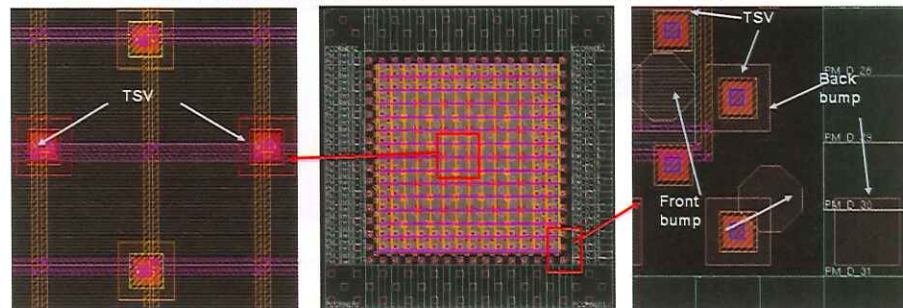


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TSV/bump generation

- Create TSV and bumps for connection with adjacent die and package
 - User could manually create TSV and bumps at defined position
 - User could create TSV/bumps with specified pattern
 - EDI could sync interface between die automatically
 - Create TSV and bumps automatically according to adjacent chips

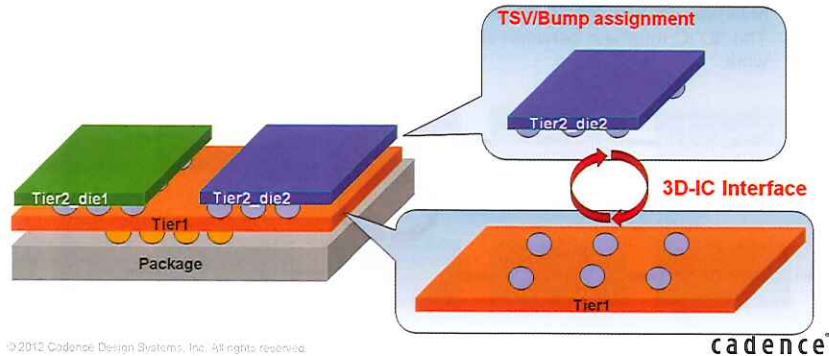


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TSV/bump assignment

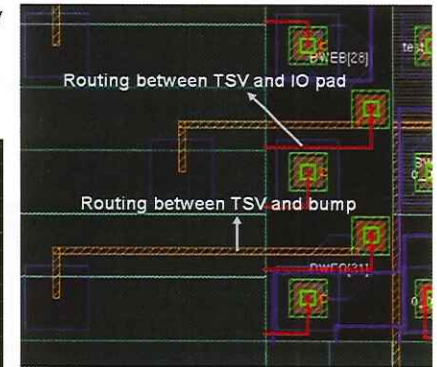
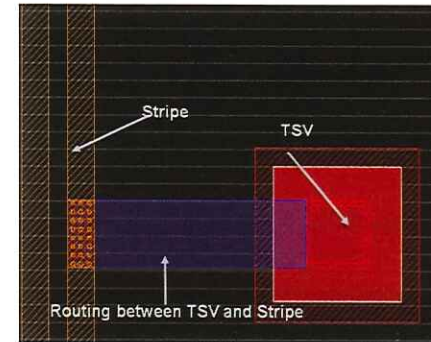
- Bumps and TSV are automatically optimized to provide optimum results (best alignment vertically, shortest wiring on each die)
 - The assignment algorithm takes into account the 3D IC top level connectivity, local connectivity and adjacent dies together to produce shortest physical connection
 - 3D IC interface are adjusted based on each local chip optimization. T
 - Change is propagated to the other die automatically or manually



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TSV/bump routing

- Routing TSV and bumps automatically
 - Route TSV to bumps
 - Route TSV to IO pads



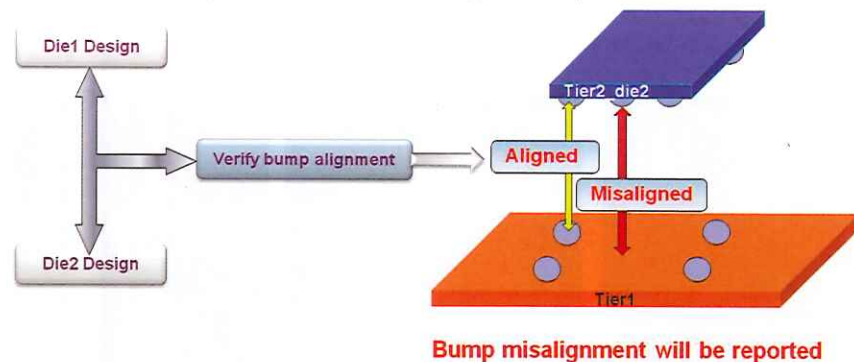
Route TSV to power stripes

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Verification

- Verify the bump alignment between chips
 - Check alignment of bumps with the same signal between chips
 - Mark misalignment on current design directly



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Combo bump

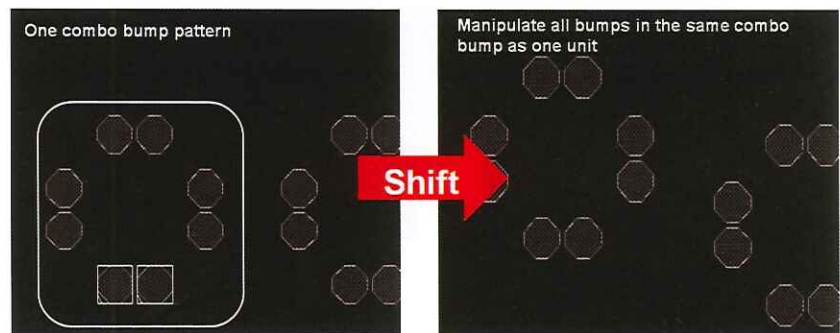
- What is combo bump?
 - A combo bump is a group of bumps that is used to pass critical signals between chips
 - A combo bump could improve design robustness
- How to support combo bump in EDI System
 - Create and assign the combo bump as one unit
 - Define routing target for the routing between combo bumps
 - Routing bumps inside combo bump with specified pattern
- Advantage
 - Keep the current 3D IC design flow while supporting full combo bump manipulations
 - Combo bump is manipulated in the same stage as normal bump
 - Maximized automatic function while manual edition applicable on all functions
 - Avoid manual work on individual bump one by one

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Combo bump creation

- Create combo bump with specified pattern as user defined
 - Provide user flexibility to edit combo bump pattern
- Manipulate all bumps in the same combo bump as one unit
 - Minimize repeated manual work on combo bump

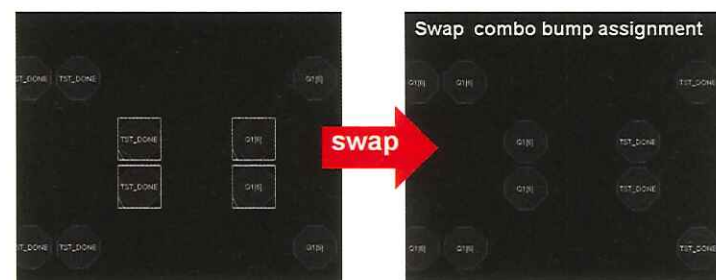


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Combo bump assignment

- Assign/unassign combo bumps
 - All bumps in the same combo bump are assigned to the same net
 - All bumps in the same combo bump will be unassigned at the same time
- Assign combo bump automatically or by user's definition
 - Assign combo bumps and normal bumps automatically
 - Assign selected combo bump to critical net
- Manipulation on combo bump assignment
 - Provide user an easy method to edit combo bump assignment

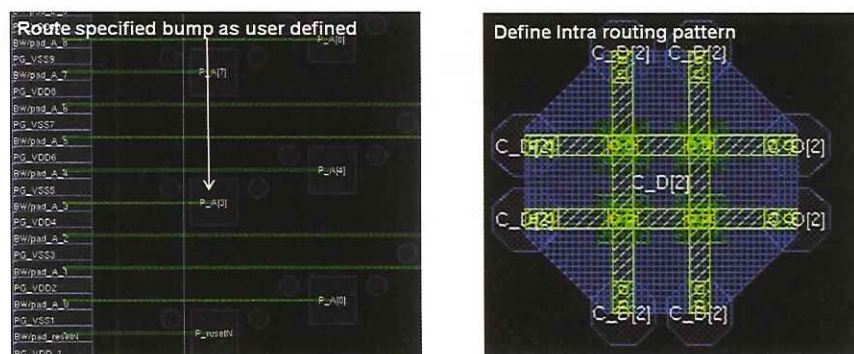


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Combo bump routing

- Routing between combo bumps and other cells
 - Define routing target in combo bump: Only specified bump will be routed to other cells
- Routing inside combo bump
 - Define routing pattern for bumps inside one combo bump



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Combo bump based 3D IC interface

- Extended the current 3D IC Interface to support micro-bumps
 - Sync up combo bump information between adjacent die automatically



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Embedded bump

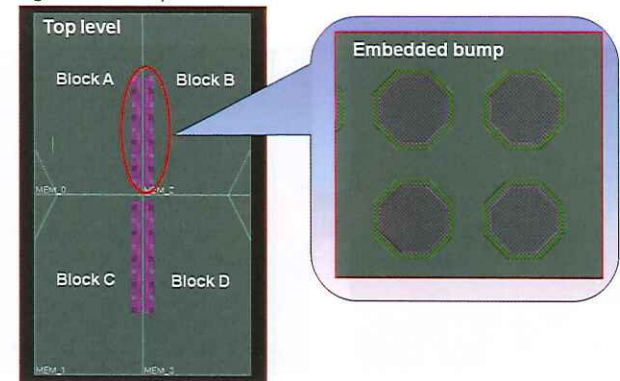
- What is an embedded bump?
 - For a bottom up design flow, all the bumps created in block level are embedded bumps
 - In the top level, tool needs to identify these embedded bump in a block and handle them as normal bumps
- Supporting embedded bumps in EDI System
 - All 3D IC commands are enhanced to identify these embedded bumps in top level
- Advantage
 - Little impact on user side
 - No special constraint for this hierarchical design flow
 - Tool will identify and handle embedded bumps automatically

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Embedded bump in top level

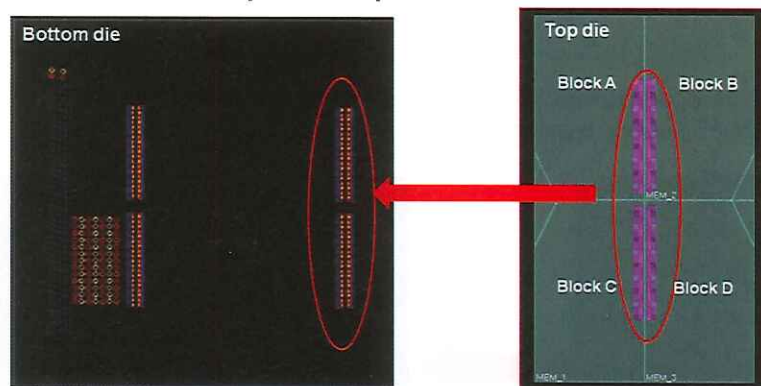
- 3D IC design flow supports combo bumps and embedded bumps
 - Treat embedded bump as normal bump during bump assignment
 - Support embedded bump during interface sync up between chips
 - Output embedded bump for downstream tools (physical verification and sign-off tools)



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Embedded bump example between two die



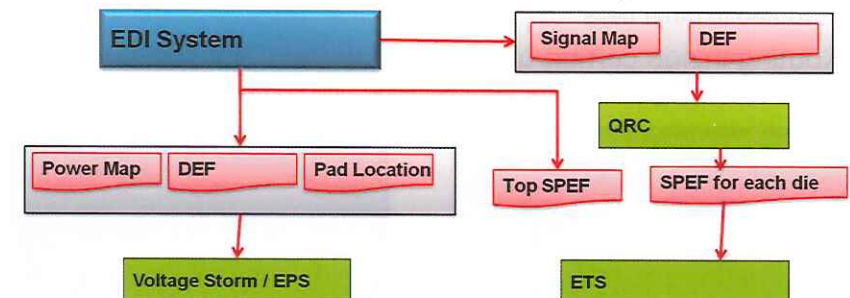
- Embedded bumps are handled the same as normal bumps during data exchange between chips
- The tool can automatically create and assign bumps on the bottom die according to the position of the embedded bump on the top die

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Export information for downstream tools

- EDI System is enhanced to export the necessary information for 3D-IC to downstream analysis tools



- In Verification and signoff stage, 3D IC is supported by
 - RC extraction
 - Static Timing Analysis
 - IR Drop Analysis

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Conclusion

- Cadence has demonstrated a solution to support the whole 3D IC design
 - The whole flow includes physical implementation, analysis and verification
- EDI has developed design flows to support physical implementation
 - Both stacked die and interposer design are supported
 - Provides automation to support multiple die stacking
 - TSV and bumps are aligned between chips automatically
 - Develop design flow to complete the Creation and routing of TSV/bumps
 - Provides necessary information for downstream analysis tools
 - Support special RC extraction to drive sign-off analysis such as EPS (Encounter Power System) and ETS (Encounter Timing System)
- Developed in close collaboration with TSMC

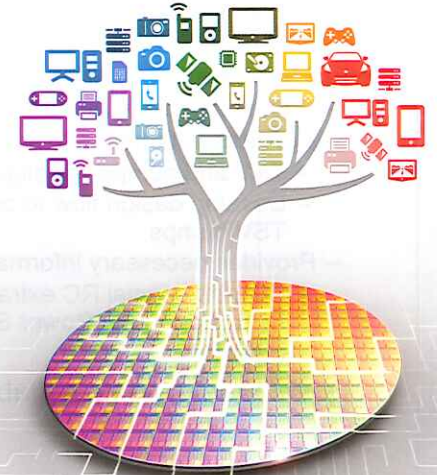
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Verification of Power, Signal, and Reliability Integrity for 3D-IC/Silicon Interposer Designs

ANSYS / Apache



ABSTRACT

Today's chip designs using 3D-IC or silicon interposer-based designs with through silicon vias (TSVs) require advanced modeling, simulation and debug capabilities in order to meet the demands of low-power mobile, high-performance computing, and consumer and automotive electronics. However, there are challenges in meeting these demands including verification of power, signal and reliability integrity. Employing a methodology flow that provides a verification platform for stacked-die designs that will meet the requirements for power, signal, and reliability is key.

From a power integrity perspective, designing the power delivery network (PDN) to multiple die becomes more challenging with TSVs, passing power from the die closer to the package on to the die higher in the stack. The use of TSVs can cause inter-die noise and other reliability issues. Here, two methods are illustrated in two different design scenarios. First, a concurrent analysis approach, where layouts of the die including the Silicon Interposer are concurrently simulated; assuming all the die data is available. The second approach is a model-based analysis, where some die data is not available, for example from an IP vendor, so a chip power model (CPM) is generated for co-analysis with the core die(s).

A power related problem exists on thermal and thermal-induced stress failures of 3D-ICs in a system environment. Multiple 3D-ICs can be put on a complex PCB in a system box. Therefore, to achieve an accurate thermal distribution on 3D-ICs, system thermal simulation should be incorporated in the power-thermal loop. Apache has developed the link between the 3D-IC package thermal simulation with the system (PCB/box) thermal simulation through the exchange of power maps per die and thermal boundary conditions for 3D-ICs. The 3D-IC thermal simulation can also interface with TSMC's thermal DDK for the thermal boundary condition.


From the signal integrity perspective, a major problem has surfaced on jitter noise analysis for wide-I/O applications on Silicon Interposer designs. Apart from the traditional SSO between package and board, the wide-I/O communication channel lays on the Silicon Interposer, where accurate RLCK channel extraction is needed with consideration for TSV modeling. The number of bits on a typical wide-I/O design can span from 1K to 8K bits in a parallel bus, which can introduce significant jitter due to simultaneous switching. The requirements for the simulation of more than one thousand bits within a reasonable amount of time also demands innovation of simulation technology. Apache has developed CIOM as a chip I/O macro-model for fast parallel bit simulation.

3D-IC/Silicon Interposer designs provide a chip-package-system platform for further integration with lower cost and higher performance. In summary, a comprehensive analysis methodology is required for power, noise, and reliability issues to ensure a timely and successful design tape-out.



ANSYS Apache Realize Your Product Promise™

Verification of Power, Signal, and Reliability Integrity for 3D IC/Silicon Interposer Designs



Fluid Dynamics Structural Mechanics Electromagnetics Systems and Multiphysics

Norman Chang, VP & Sr. Product Strategist

Apache Design, a subsidiary of ANSYS

ANSYS Outline

- **Benefits of Silicon Interposer Designs**
- Multi-die Power Integrity Need
- Chip-Package-System Thermal Co-analysis
- Wide-I/O SSO Jitter Analysis
- Summary

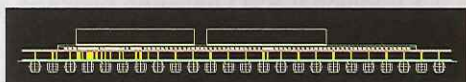
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ANSYS **Benefits of Silicon Interposer Designs**

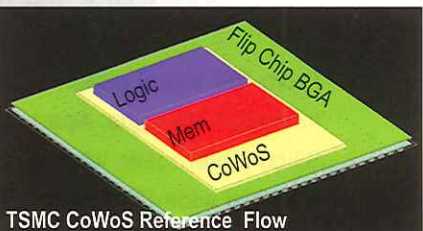
- **Small form factor with economical packaging**
 - Driven by continuous demand for smaller/faster/higher design integration at a lower cost
 - Enhanced system performance (higher bandwidth and lower power) via high density interconnect
- **High-performance wide-I/O connections to RAMs**
 - Shorten interconnection from chip-to-chip via Silicon
 - Low driver/receiver power: Interposer C << package C
- **Good fit to silicon process technology**
 - TSV independent of technology nodes, decoupled from platform technology
 - Lower cost organic substrate

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ANSYS **TSMC CoWoS™ Design Example**

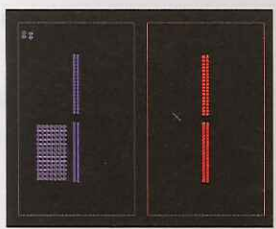


Side View

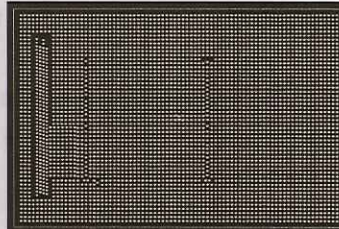


Flip Chip BGA
Logic
Mem
CoWoS

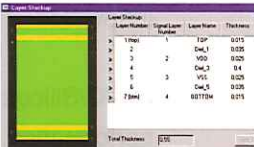
TSMC CoWoS Reference Flow



Micro-bumps for Logic and Mem. Dies



Bumps for CoWoS



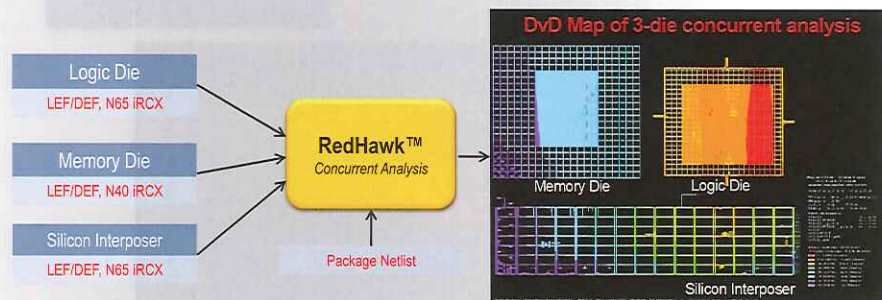
Substrate Section

Layer	Material	Thickness
1	OSP	0.015
2	Die_1	0.025
3	Die_2	0.025
4	Die_3	0.04
5	Die_4	0.025
6	Die_5	0.025
7	Die_6	0.015

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ANSYS Concurrent Multi-die Voltage Drop Analysis

- Input multiple-die design and corresponding process data (can be of different technologies), all at once
- Impact from shared P/G nets and de-cap in interposer die can be factored into memory and logic die

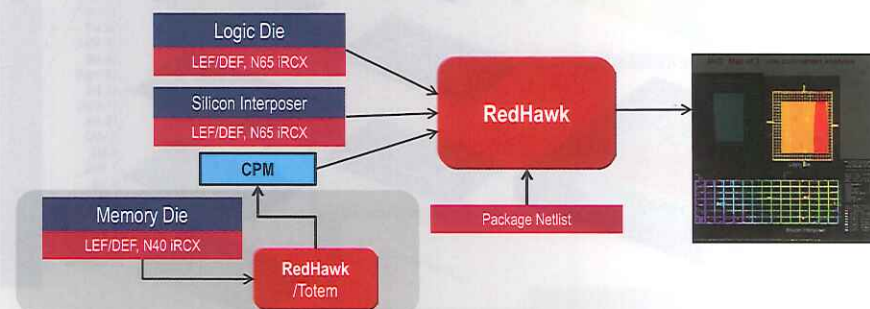


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ANSYS CPM-based Multi-die IR/DvD Analysis

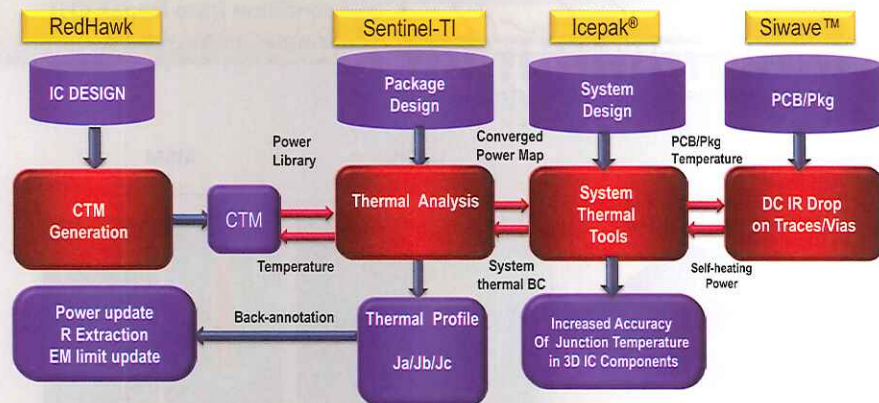
- Suitable when one die is external without the complete design database
- Chip Power Model (CPM™) is a die model with R/L/C network and current profile, generated by RedHawk or Totem™
- Enables simple hand-off and fast turn-around-time



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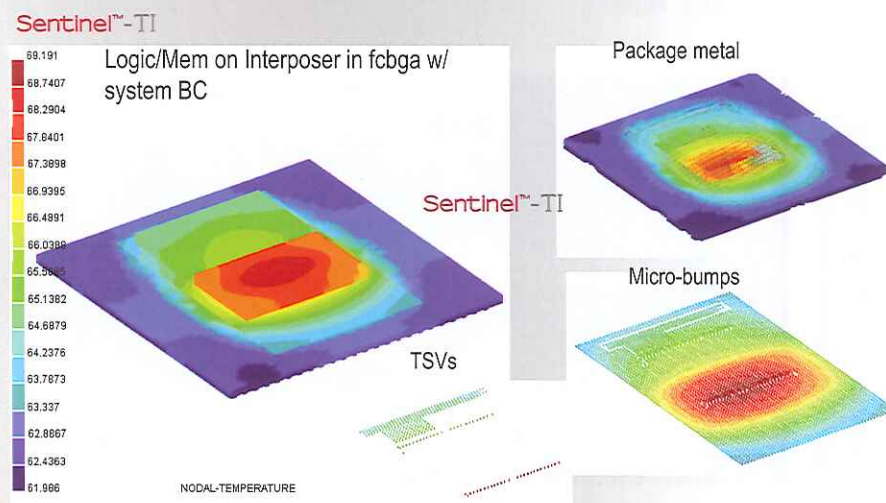
ANSYS Flow Integration of CTM, Sentinel-TI and Icepak/Siwave in Chip-Package-System Thermal Co-analysis



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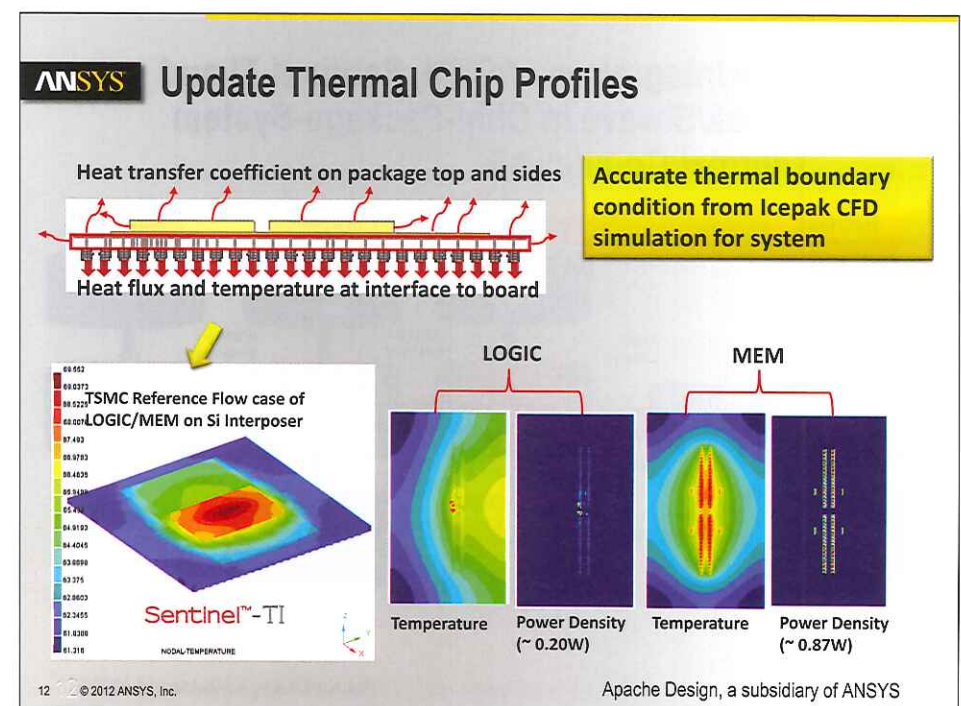
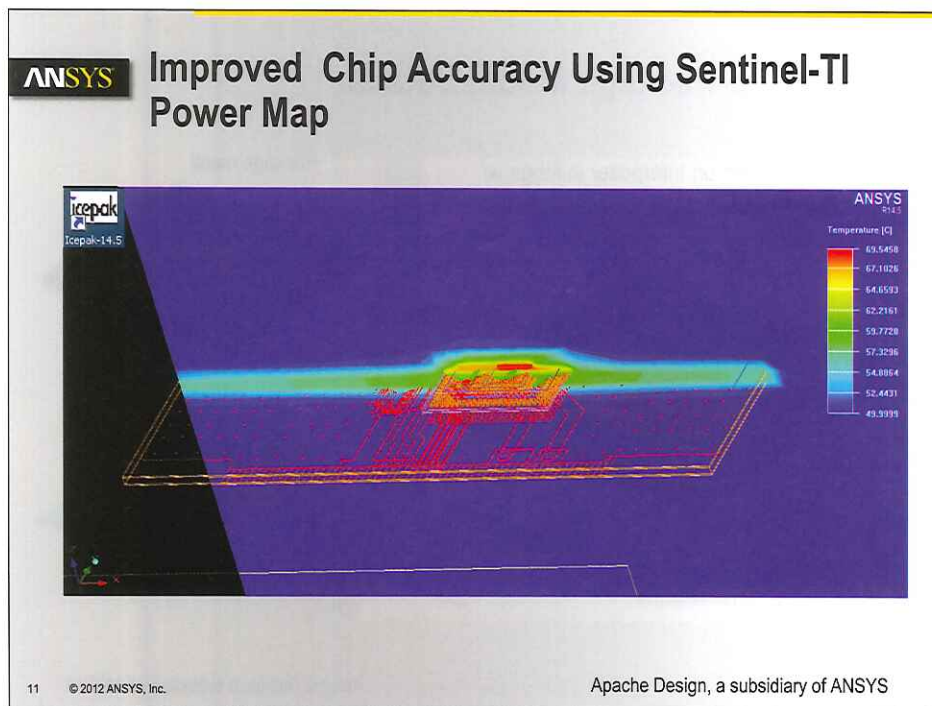
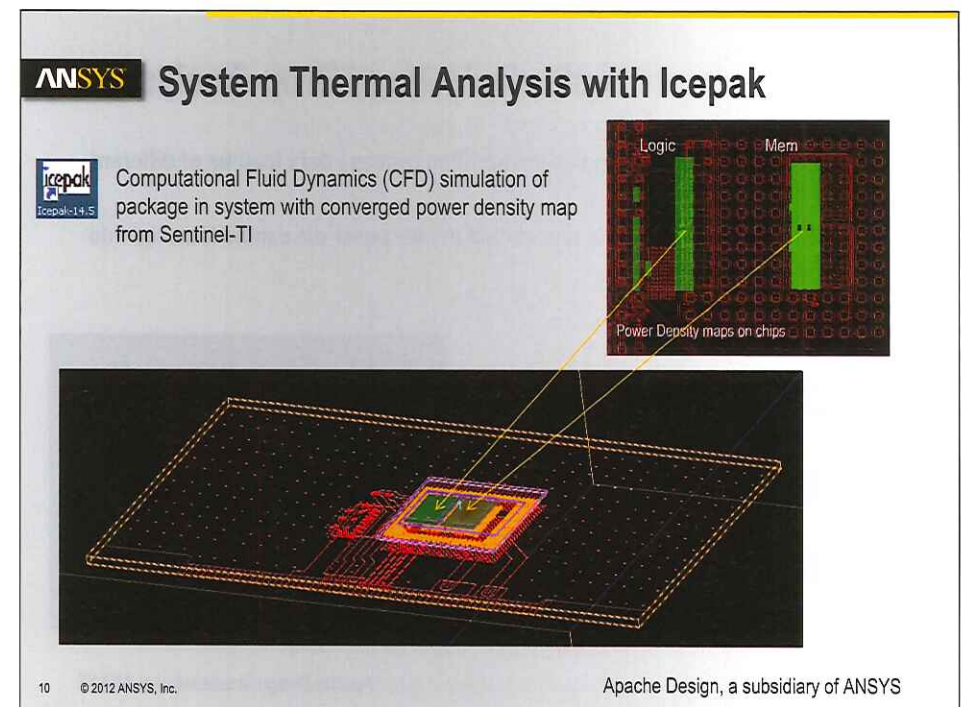
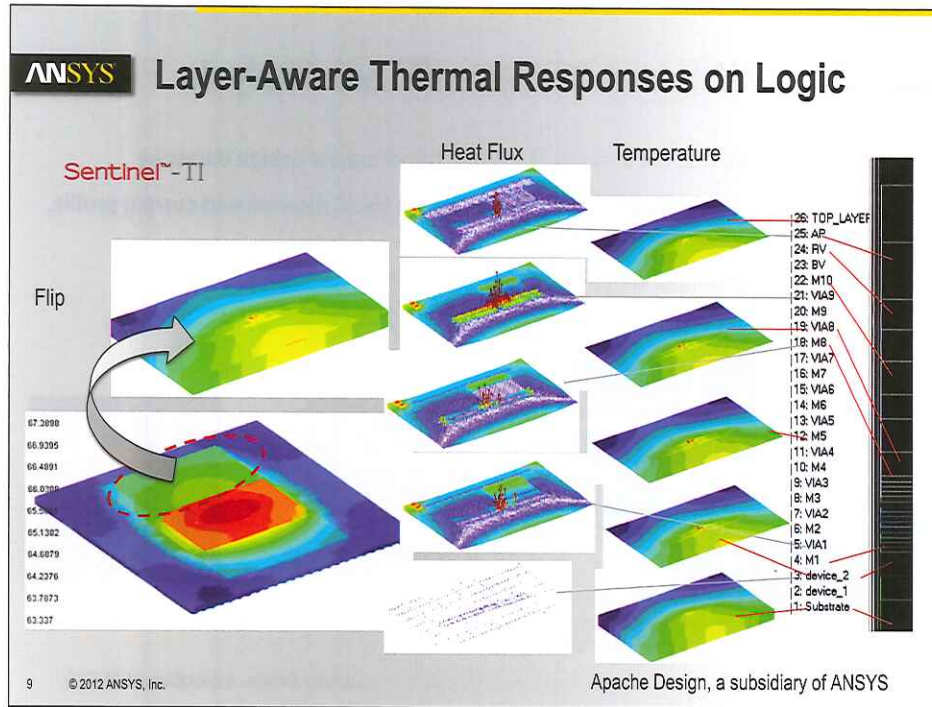
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ANSYS Chip-Package Model Details



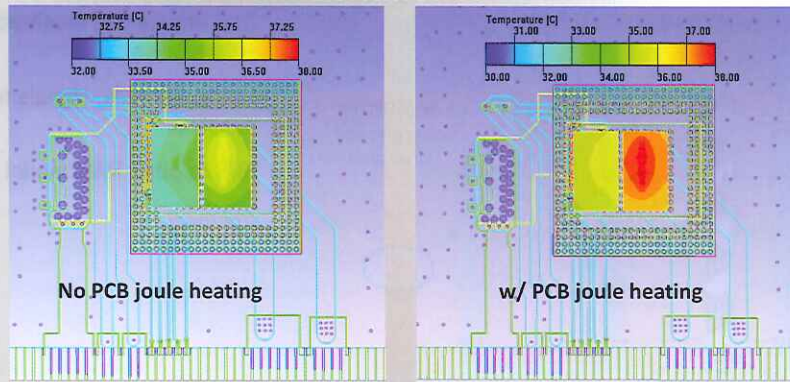
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Temperature Profile w/ Joule Heating Calculation in SI-wave based on C4 Bump Current from Sentinel-TI



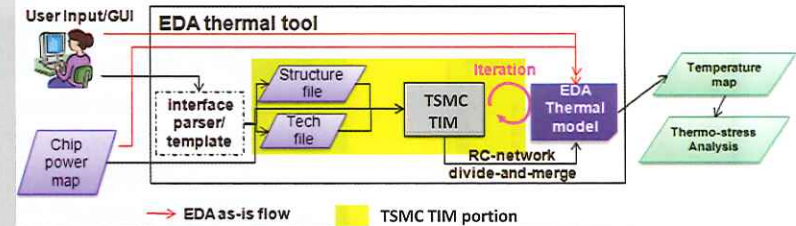
- Ref. Flow CoWoS board and package simulated in forced convection JEDEC chamber with flow velocity =1 m/s
- System ambient temperature = 20C
- Temperature rise by 1.5C on Memory (7.5% increase) when self-heating included

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Sentinel-TI in TSMC TIM Flow for Chip-Package-System Thermal Co-analysis



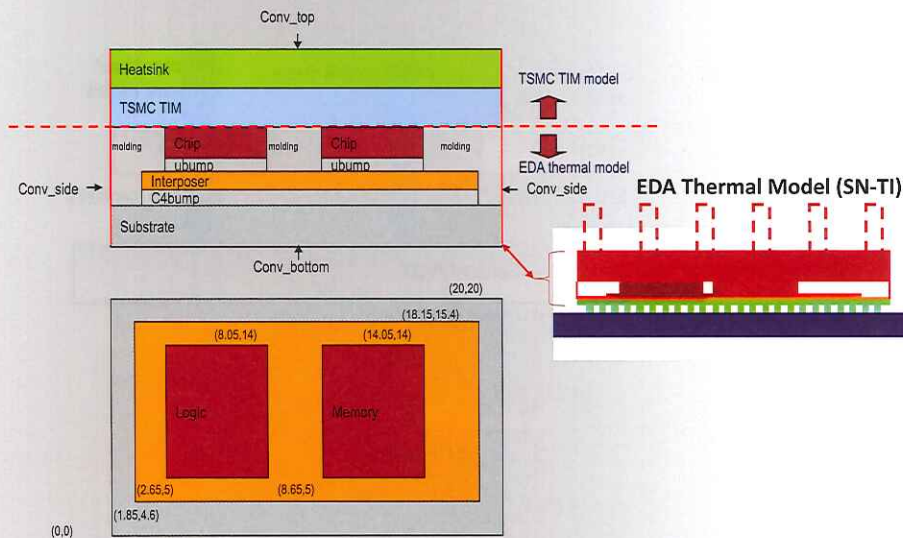
- Step 1.** Sentinel-TI generates and support TSMC TIM input files (struct.txt and tech.txt) and chip power map
- For use by TSMC TIM utility to generate thermal model
- Step 2.** Sentinel-TI generates TSMC TIM thermal model and performs thermal analysis
- Includes the thermal model in analysis and export temperature map at die heating faces

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Test Case: Logic + Memory on Interposer

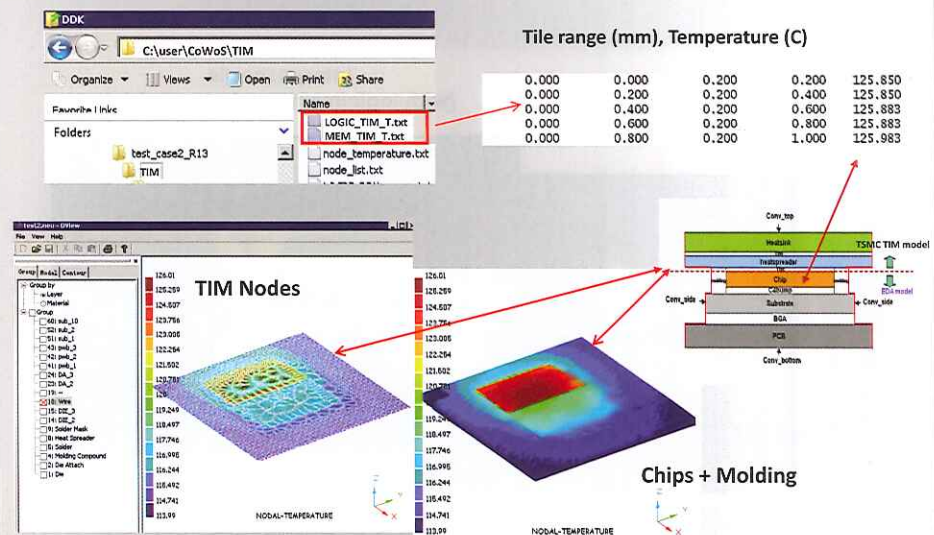


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Tile-based Die Temperature

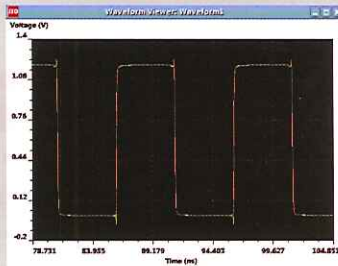


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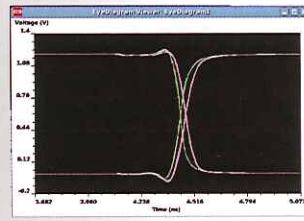
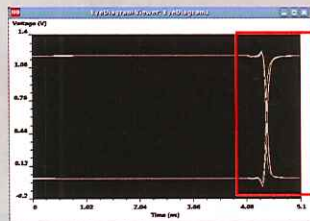
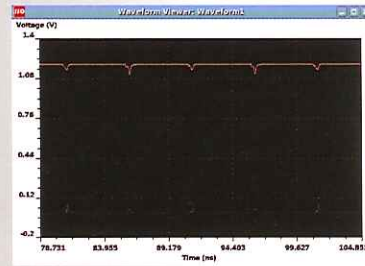
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ANSYS Wide-I/O SSO Eye Diagram Results

Signal Waveforms



PG Waveforms



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ANSYS Summary

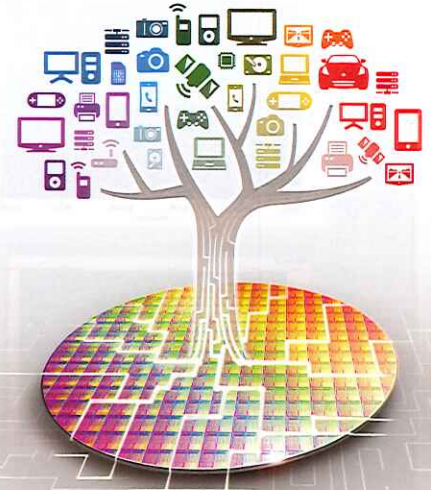
- Power integrity analysis on TSMC CoWoS design can be achieved through CPM-based or concurrent analysis
- Chip-Package-System (CPS) thermal analysis is demonstrated with integrated CPS thermal tools or interfaced with TSMC TIM thermal boundary condition
- Wide-I/O with CoWoS is becoming a major platform for high-performance logic<->memory designs
 - Wide-IO channel jitter analysis is illustrated

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TSMC Certification for Cadence 20nm RTL-to-GDSII Flow

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ABSTRACT

As part of the TSMC 20nm process rollout, Cadence has been working closely with TSMC to certify the Cadence solution for TSMC 20nm.

This paper focuses on the certification of the Cadence RTL-to-GDSII methodology for TSMC's 20nm process. The paper will present the certification steps that took place, timelines for major milestones, and cover the new considerations for 20nm in the RTL-to-GDSII methodology, together with flow metrics that were achieved during the certification process.

Specific topics of interest in this paper include double patterning considerations for and routing, multi-value SPEF extraction and timing analysis, new DC/AC electromigration analysis requirements and other topics.

In short, the paper will provide the audience an overview of the Cadence 20nm RTL-to-GDSII methodology steps as certified by TSMC.



TSMC Certification for Cadence 20nm RTL-to-GDSII flow

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TSMC-Cadence 20nm Certification Overview

- A collaboration between TSMC and Cadence resolves P&R flow challenges in 20nm process node.
- Addresses 20nm design challenges :
 - 20nm double patterning routing
 - New design rules defined in TSMC 20nm DRM
 - Double patterning area efficiency
- Goal: Providing Cadence-TSMC customers a faster path to 20nm silicon success



Cadence Encounter and Virtuoso Design Platform are certified at TSMC 20nm for DRM 0.9

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20nm Challenges

- New DRC rules
- Double patterning requirements
- Dominant wire delay/variation effects
- 100M+ instances for large designs
- Turnaround time
- Increasing complexity, potentially more costly runtime impact of errors
- More aggressive PPA expectations
- GHZ-range clock frequencies
- RTL-to-GDSII timing convergence

“Concurrent” Performance, Power and Area Optimization
GigaOpt and clock concurrent optimization

“Giga Scale” Design and Productivity
GigaFlex technology

Silicon Manufacturability & Variation
20nm DPT-correct methodology

TSMC 20nm Certification focus

Encounter 20nm RTL-to-Signoff Flow DPT-correct physical implementation and signoff

20nm rule support,
FlexColor DPT-correct
placement and routing

DPT Placement

DPT Routing with
NanoRoute

Mask-shift accuracy with
multi-value SPEF

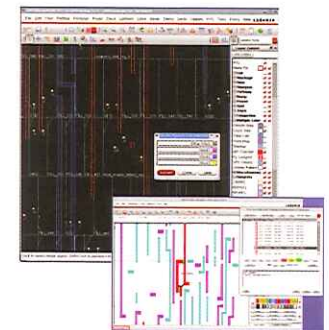
RC extraction with 20nm
and DPT support

Advanced timing
modeling and DC/AC
EM analysis

Timing and power
Signoff

Golden physical signoff
with auto-fixing

Physical/DFM Signoff
DRC, DPT checks

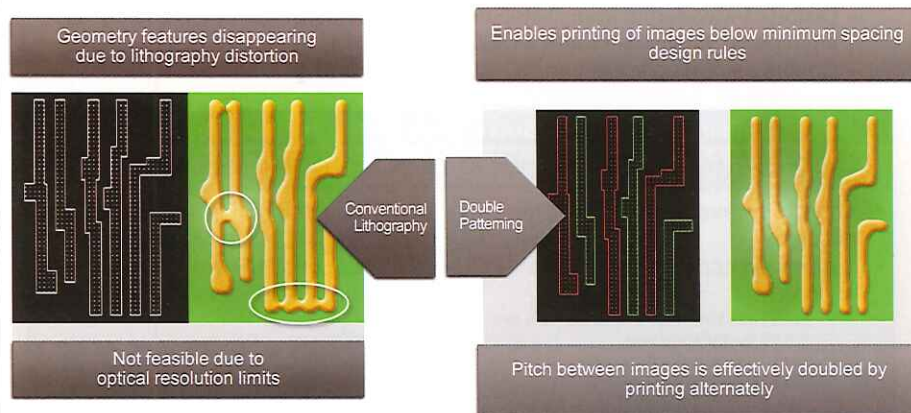


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Double patterning

A “must-have” for wire pitches smaller than 80nm

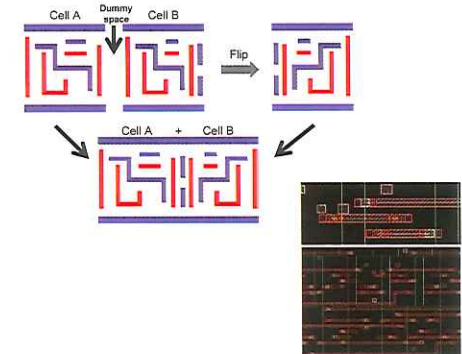


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FlexColor DPT Placement and Routing in EDI System

- 20nm correct-by-construction DPT enabled in placement, optimization and routing.
- Full 20nm DRC and DPT-correct methodology ensures optimal routability and QoR.
- Supports DPT same color and different color rules
- Cell/IP colorization for ports and obstructions



Correct-by-construction approach improves area efficiency and enables ECO changes effectively

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20nm Extraction, Timing and Power Signoff



*Note: Cadence Liberate created standard cell Liberty views

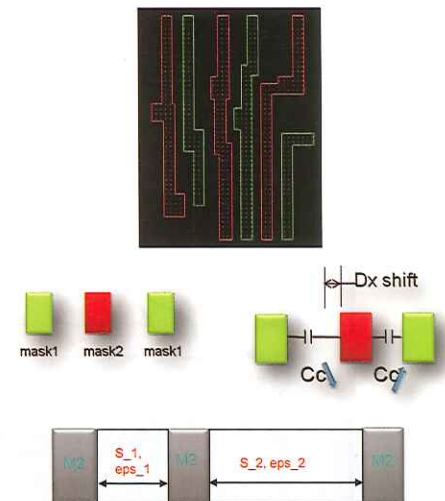
- CCS/ECSM timing, noise, power
- Enhanced ECSM models for improved timing accuracy
- 8 piece ECSM pin capacitance
- Partial voltage swings
- Increased ECSM waveform voltage range (2%-98%) from (5%-95%)

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20nm DPT Extraction Challenges

- DPT causes potential misalignment between the two masks of the same layer
- Misalignment is a random variation that impacts circuit performance
- Mask shift challenge
 - Explosion of process corners to capture Tcap variations
 - New modeling requirements to address cap. variations



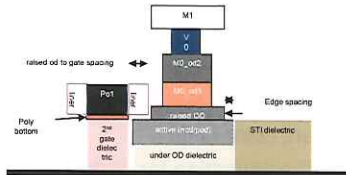
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Extraction: TSMC 20nm QRC Certification

- DPT Shift Effect modeled as spacing dependent dielectric constant (intra metal dielectric)
- DPT corner with multi-value SPEF value output
- DPT color import to QRC with LEF/DEF 5.8 syntax from EDI
- Reduced pessimism multi-value SPEF value output based on EDI color
 - Mask shift capacitive effect removed if two wires are same color

New extraction considerations at 20nm
2-step M0/V0, Raised source-drain with bias, 3D fringing etc



QRC is certified at TSMC 20nm for SPICE 0.1 and 0.5

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Timing Analysis: TSMC 20n Encounter Timing System Certification

- 20nm timing analysis challenges
 - Distorted waveforms from Distributed RC, Back-Miller current, crosstalk and input noise, nonlinear characteristics of gates
 - Double patterning impact on RC extraction for timing

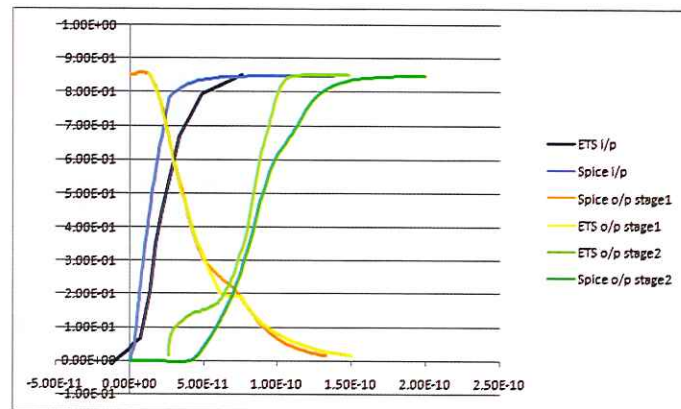
ETS Enhancements to address 20nm timing analysis challenges

Waveform effect modeling enhancements	Double patterning-correct extraction support
<ul style="list-style-type: none"> • Improved waveform modeling for accuracy • 8-piece pin capacitance models support <ul style="list-style-type: none"> • 90% 70% 50% 40% 30% 20% 10% and 0.01% for fall transition • 10% 30% 50% 60% 70% 80% 90% and 99.99% for rise transition • Support for pre-driver waveform inclusion in the library. 	<ul style="list-style-type: none"> • Multi-valued SPEF from Double patterning RC extraction • ETS supports timing analysis using multi-Value SPEF for early/late paths

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ETS 20nm Delay Calculation Accuracy w.r.t Spice with Waveform Effect Modeling



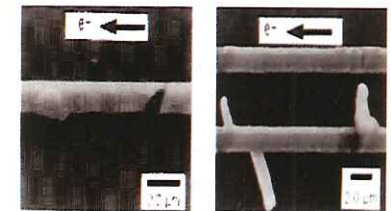
ETS is certified at TSMC 20nm for both base and SI delay

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DC/AC Electro-migration Analysis in EPS

- What is Electromigration (EM) Analysis?
 - EM is the mass transport of a metal due to the momentum transfer between conducting electrons and diffusing metal atoms. It can cause opens or short
 - EM force is directly proportional to the current density in the metal route.
 - DC and AC current limits are defined for every metal and via/contact layers.



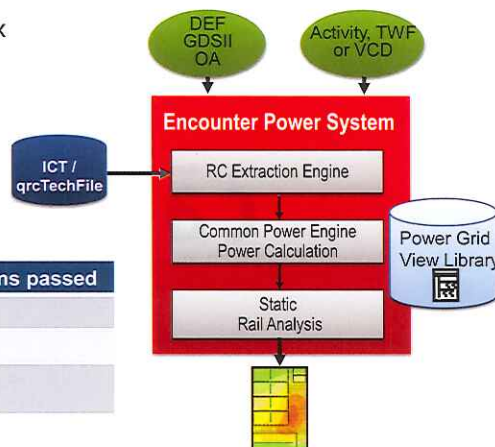
a) Open circuit failure, b) Hillocking, short circuit failure. (W. D. Nix et al., 1992)

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Electromigration analysis: TSMC 20nm Encounter Power System Certification

- Support for basic and complex topology dependent EM rules
- EM models from ICT section within qrcTechFile
- EM model tied to qrcTechFile
 - Synchronized and correct metal options



EPS Electromigration certification items passed

Current probes on nodes

DC and AC electromigration calculation

Effective resistance calculation

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20nm Implementation and Signoff Physical Verification

Physical Implementation

Built-in DRC engines, correct-by-construction DPT approach

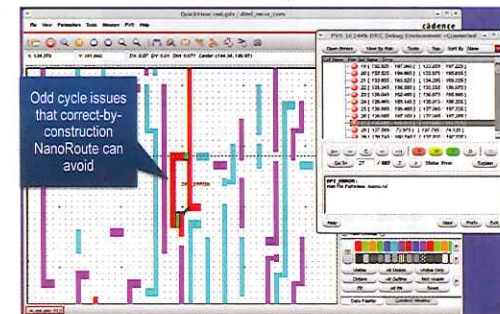
Physical/DFM Signoff

Golden check Auto-fixing enablement

Tapeout

20nm physical signoff

- Accurate DRC checks and color conflict loop detection DPT checks
- Auto-fixing with NanoRoute in EDI System
- Same physical verification engine used in Virtuoso custom design

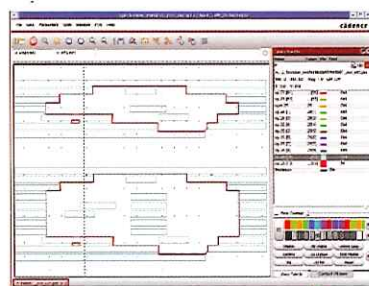


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Physical Verification: TSMC 20nm PVS Certification

- DRC/DPT is qualified with DRM versions.
 - Support for delta voltage dependent spacing checks and ac
 - Support for G0 rules and compliance check
 - Support for pre-coloring and partial 2-coloring violation outp
- Virtuoso IPVS is certified with DRM versions
 - Support for real-time G0 rules and compliance checks
 - Support for real-time pre-coloring check
- LVS/LPE is qualified with DRM versions
 - Supports for iLVS support with WOSE and PMET2

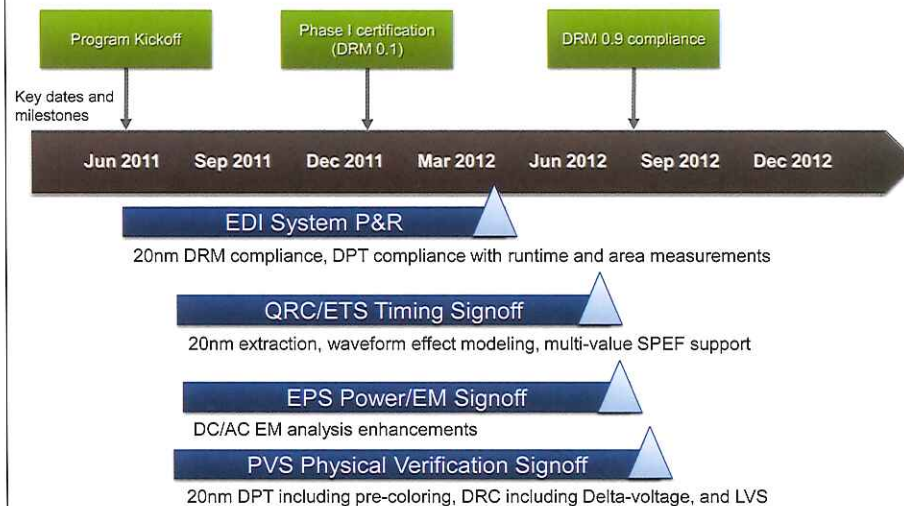


PVS is qualified at TSMC 20nm for DRM 0.9 and SPICE 0.5
Deck is available for customers

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TSMC-Cadence 20nm Certification Timeline and Milestones



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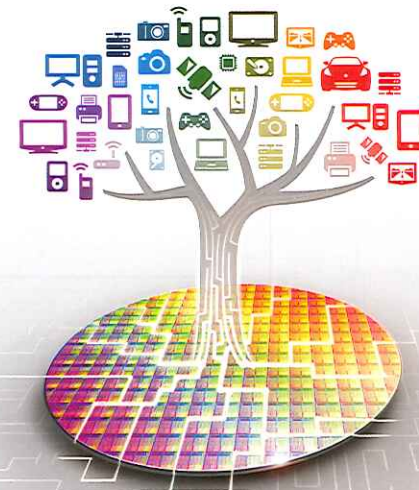
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Double-Patterning Technology and Impact on 20nm Designs

Synopsys

ABSTRACT

Double patterning technology (DPT) has emerged as a critical technique for ensuring printability of device and interconnects layers in 20nm IC manufacturing. DPT provides an attractive alternative to more expensive lithography options, but it introduces new challenges in parasitic extraction and timing signoff analysis due to increased variation from multiple exposures. In his talk, Bari Biswas will present an overview of the double patterning technology and discuss DPT aware modeling and extraction in Synopsys' StarRC extraction solution, developed in close collaboration with TSMC. The presentation will cover both digital and custom design flows targeting TSMC's 20nm process node and will also include a preview of the future 3D modeling capabilities for next-generation design.

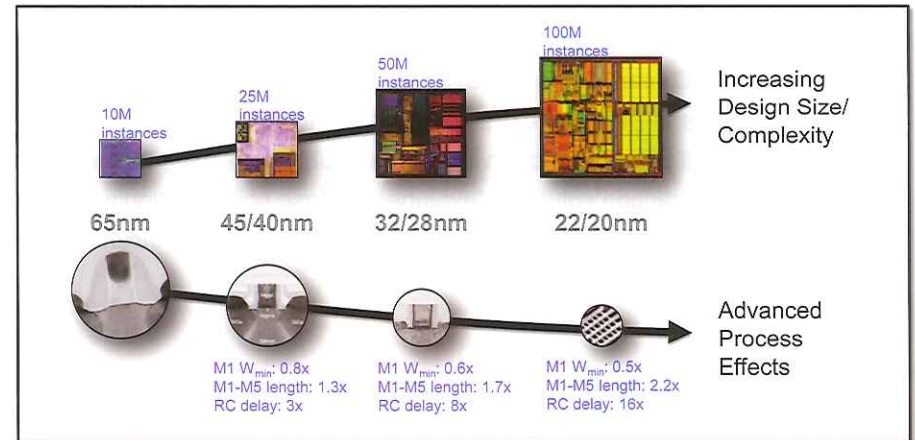


Double-patterning Technology and Impact on 20-nm Designs

TSMC OIP Ecosystem Forum

Bari Biswas
Sr. Director, R&D

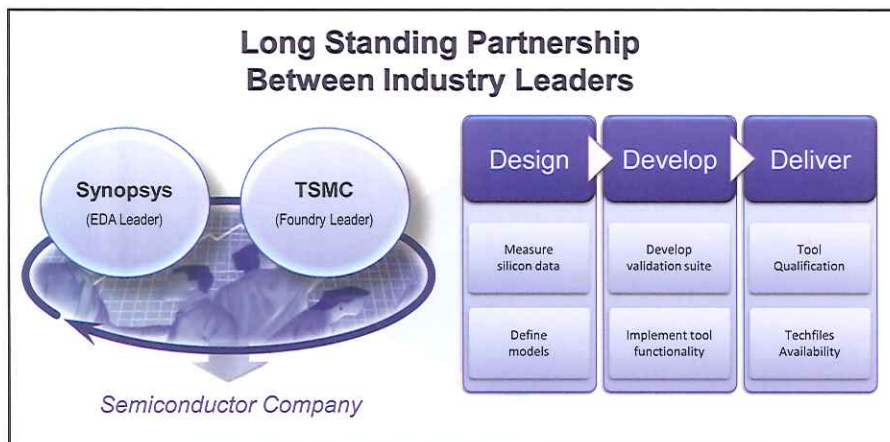
Gigascale Design Challenges



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Strong Collaboration Driving Success

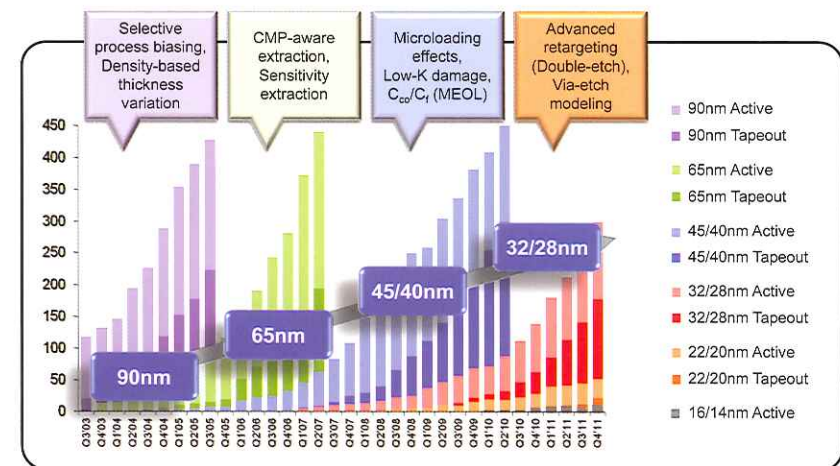


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The Technology Progression

Advanced Process Modeling Driving Silicon Success



Source: Synopsys Global Technical Services

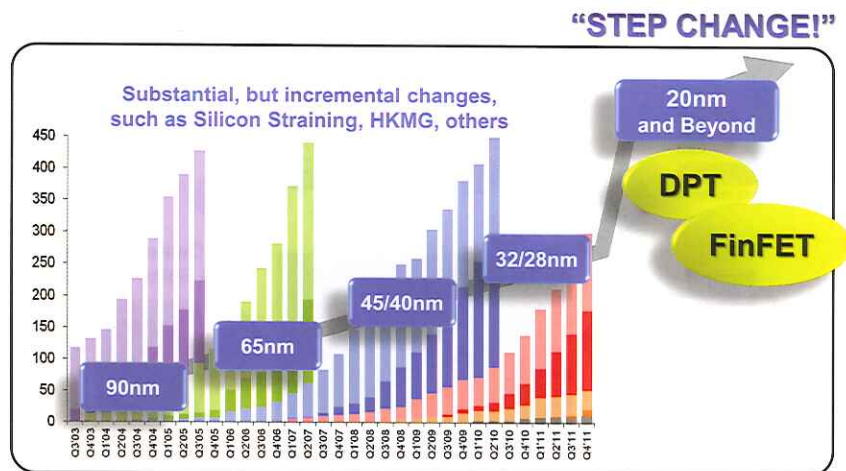
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The Technology Progression

Advanced Process Modeling Driving Silicon Success



Source: Synopsys Global Technical Services

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Double Patterning

“Someday, chips might be made with X-rays. Until then, double-patterning lithography will be the only game in town...”

Chris A. Mack, IEEE Spectrum, November 2008

A Little Bit of Lithography Math!

$$\text{CD} = k_1 \left(\frac{\lambda}{\text{NA}} \right)$$

Half-Pitch

CD: Critical dimension
K1: Process coefficient
 λ : Wavelength of light
NA: Numerical aperture of lens

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A Little Bit of Lithography Math!

$$\text{CD} = k_1 \left(\frac{\lambda}{\text{NA}} \right)$$

Half-Pitch

Limit of single patterning:

Pitch of **~72nm**

- Shortest Wavelength (λ) = 193nm
- Highest NA = 1.35
- Lowest theoretical limit of K1 = 0.25

Smallest pitch at various technology nodes

80nm (at 22nm) and 64nm (at 20nm)

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Double Patterning Basics

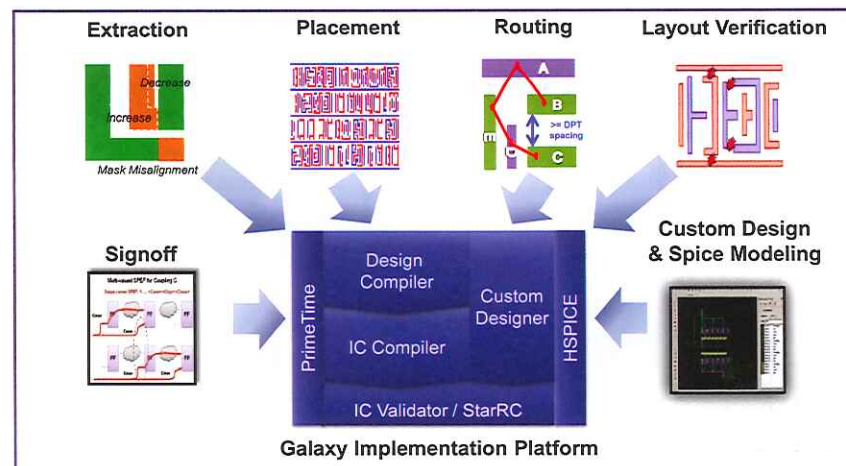
- Double Patterning = Print twice → Two masks
 - Enables higher K1, less aggressive RET and better printability
 - Higher cost, but cheaper than Next Generation Lithography (NGL)



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Synopsys 20nm DPT-Aware Solution StarRC a Key Component of Galaxy 20nm Solution



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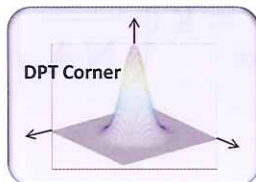
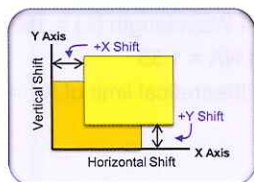
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DPT and Mask Shift Misalignment

Non-zero mask misalignment from two separate exposures: Shift is random – die to die, wafer to wafer

Variation modeling using DPT corner: Each traditional corner “modified” to incorporate DPT effect e.g., cworst_ccworst



Bounding Approach (DPT corners)

- Modification of current parasitic corners to incorporate DPT effects
- Support pre-coloring for sensitive nets, IP ports etc.,

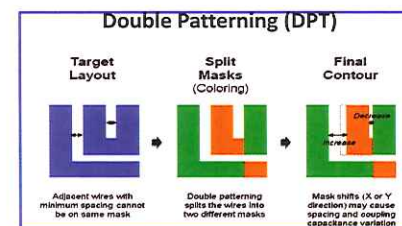
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DPT Modeling in StarRC

- Mask misalignment issue
 - Mask can shift in x and y directions, causing capacitance variation
 - Same layer next neighbor lateral edge cap variation more prominent



- Parasitic variation modeling using “additional” DPT corners
 - Model lateral cap variation using ER_VS_SI_SPACING in ITF (Tech-file)

StarRC DPT Corner Modeling

```

DIELECTRIC <dielectric_name> {
  ...
  THICKNESS = <value>
  ER = e0
  ER_VS_SI_SPACING {
    (S1, ER1) (S2, ER2) (S3, ER3) .... }
}

```



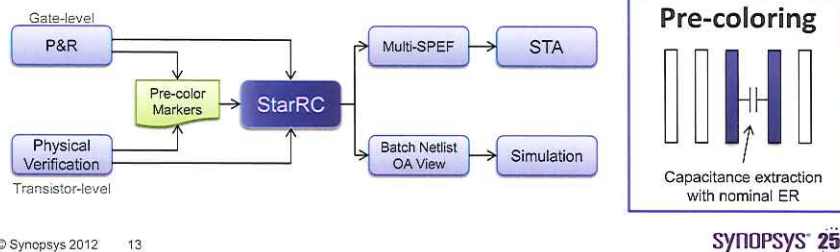
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Pre-Coloring Support with DPT Corners

Expression of designers "mask litent"

- Motivation: Reduce mask-to-mask variation
 - Allow "pre-color" of specific critical nets (e.g., differential pairs, clocks) and force them to be on same mask
- StarRC pre-coloring support
 - Color markers in separate GDSII file or embedded in input database
 - Capacitance between same color polygons extracted with nominal ER
 - Capacitances between other polygons extracted with ER_VS_SI_SPACING table (min, max)



Support for TSMC 20nm Process Corners

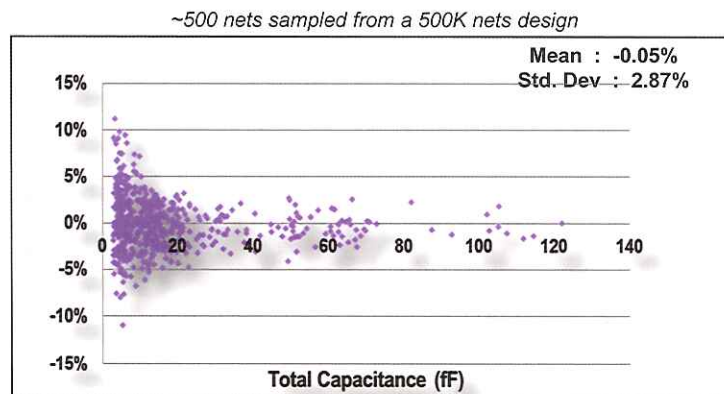
- Five basic corners, modified to incorporate DPT effect
 - typical, cworst_ccworst, cbest_ccbest, rcworst_ccworst, rcbest_ccbest
 - Minimal changes to customer's design flow
- Additional six corners for advanced analysis
 - To support multi-value parasitics and pre-color flows
 - Triplet for typical corner (typical_ccworst and typical_ccbest)
 - Nominal settings for corners (cworst, cbest, rcworst, rcbest)
- Total of 5 corners with 11 tech files available at TSMC online

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StarRC Accuracy vs. Field-Solver

TSMC 20nm Process with DPT Corners



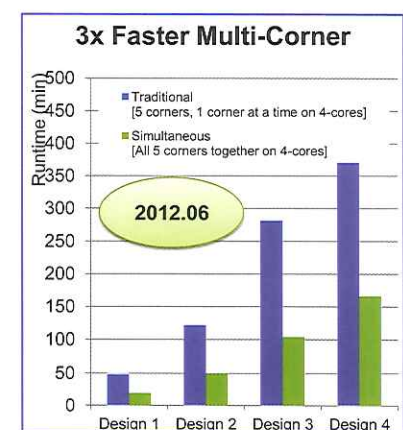
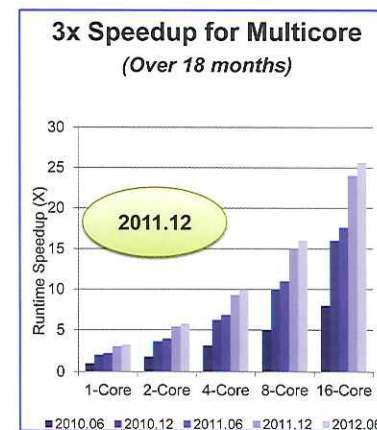
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Performance and TAT Improvements

"Must-have" for increasing design sizes at 20nm & below



Fastest sign-off extractor in the market today !
Product Roadmap: Deliver 2x faster every 2 years

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Summary

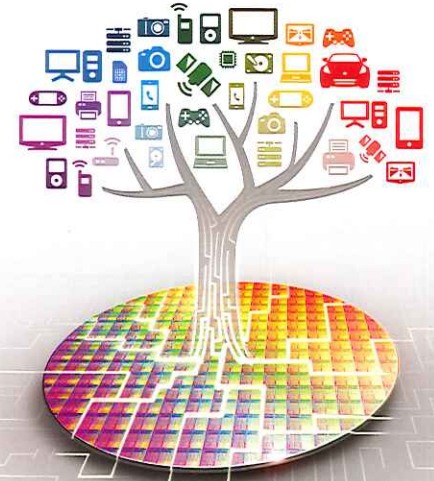
- DPT is an attractive alternative to other expensive lithography, however mask mis-alignment requires additional modeling
- Close collaboration between TSMC and Synopsys delivering innovative DPT solution to model cap variation using corner-based approach and including pre-coloring
- For further information:
 - Contact: Shekhar Kapoor, Marketing, skapoor@synopsys.com

NOTE

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Improved Design for Reliability Using Calibre PERC

Mentor Graphics

ABSTRACT

Verification of 20nm designs is expected to bring significant challenges. A robust verification methodology that addresses circuit reliability is increasingly difficult. At 20nm, new devices that incorporate thin oxides are less robust and more subject to electrical overstress (EOS) failures. The increased use of mixed-signal and multi-voltage design techniques also increases the likelihood that transistors could be implemented in an incorrect voltage domain. Preventing long term electrical failure means IC designers should utilize new techniques to validate ESD structures, protect against EOS, manage multiple power domains, and carefully balance sensitive analog circuits. This session describes these challenges and how MediaTek is using Calibre PERC to address IC design for reliability issues

A vibrant, abstract illustration of a building facade. The image features a grid of windows, some with red and orange patterns, and a large, stylized 'T' shape in the foreground. The colors are bright and saturated, with a mix of purple, yellow, orange, and red. The style is reminiscent of a stylized, colorful photograph or a graphic design.

October, 2012



Figure 1 illustrates Design Intent Validation, showing two main components: Low Power and Design Symmetry.

Low Power: This section displays a circuit diagram with two 'LAMB' blocks connected to an 'M' block, and a schematic of a differential pair with a current source 'I' and a label 'm2'.

Design Symmetry: This section displays a schematic of a differential pair with a current source 'I' and a label 'm2', and a schematic of a differential pair with a current source 'I' and a label 'm2'.

Calibre PERC

ESD
Avoid Chip Failures

EOS
Avoid Chip Failures

Voltage Aware DRC
Realize Area Savings

Verification beyond traditional DRC, LVS and ERC



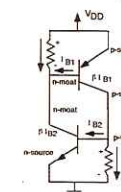
http://p32.vitalfiles.wordpress.com/2010/11/022_6.jpg
http://2.bp.blogspot.com/_9XrYGA0907/1w78b3c_2JIAAAAAAAAAAUC/AAAAAAAAAAQ/6w5o1600/Back_Lucine_body_structure_Structural.jpg
<http://www.immucore.com/tair/bp/images/default.asp?img=/www.immucore.com/images/capagag-serverfarm.jpg>
http://en.wikipedia.org/wiki/File:Galaxy_Nexus_smartphone.jpg
http://www.podsz.org/wiki/File:Sony_PSP-1000-Body.png
<http://www.comunity.com/wp-content/uploads/2011/10/gmc-terram-active-safety.jpg>

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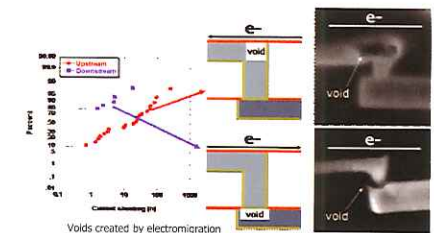
- Time Dependent Dielectric Breakdown (TDDB)
- Negative Bias Temperature Instability (NBTI)
- Hot Carrier Injection (HCI)
- Threshold Voltage shift (V_t)
- Electromigration (EM)
- Electrical Overstress (EOS)
- Latch-up
- Others



Damage to input pin due to electrical overstress (EOS) during post-programming burn-in at a third-party test house



P.
la



Voids created by electromigration

Solving Reliability Issues Comprehensive Coverage

- Develop solutions that remove doubt
 - Provide deterministic checking to eliminate errors
 - The "human" element is often the weakest link

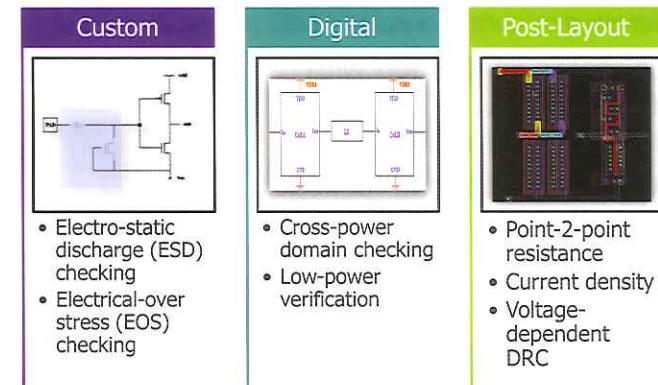
Items	Calibre PERC	Marker Layers	Eye Ball
Rules Coverage	over 90%	under 30%	under 10%
False Error	no	many	always
Tool Integration	Topology, LVS, DRC, R-extraction	DRC + manual marker	manual examination
Tool Quality	sign-off level	dependence	no quality
Programmable	fully	partially	never
Run Time	minutes	minutes ~ hours	hours ~ days
Human Error	never	sometimes	always
User Usage	automatic	semi-auto	manual

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Circuit Verification Aspects

- Electrical checks using PERC are critical for comprehensive circuit verification

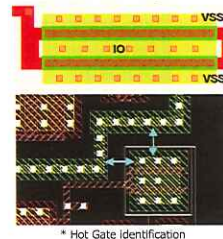
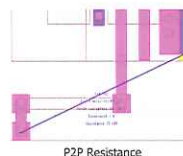
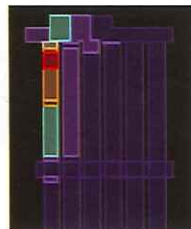
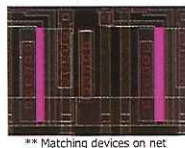


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Solving Reliability Issues Layout Centric Verification Challenges

- Transistor placement and design interactions can have significant impact on design robustness
 - Point 2 Point resistance (P2P)
 - Current Density (CD)
 - Hot gate / diffusion identification
 - Layer extension / coverage
 - Device matching
 - DECAP placement
 - Forward bias PN junctions.
 - Others



* T. Shrivastava, et al., "A DRC-Based Check Tool for ESD Layout Verification", ESD:ESD 2009, pp 44-2-1 - 44-2-9

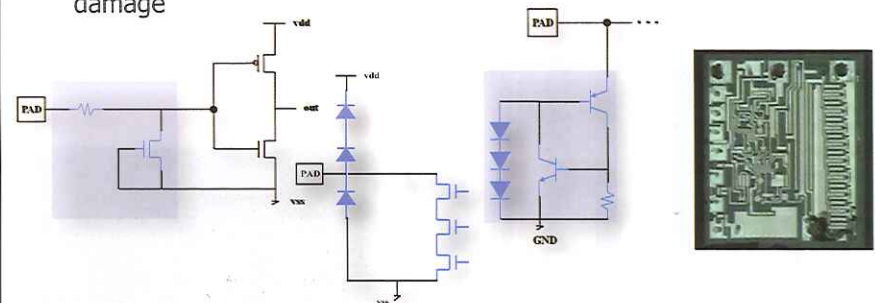
** P. Gibson, et al., "A Framework for Logic-Aware Layout Analysis", DQED 2010, pp171-175

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ESD Design Rules

- Electrostatic discharge (ESD) causes severe damage to ICs
- Several protection schemes have been proposed to mitigate this damage



Checking for proper ESD protection circuits is needed for reliable design

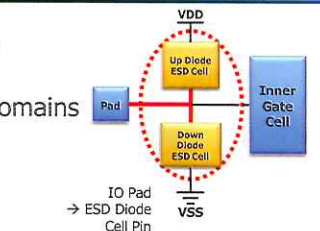
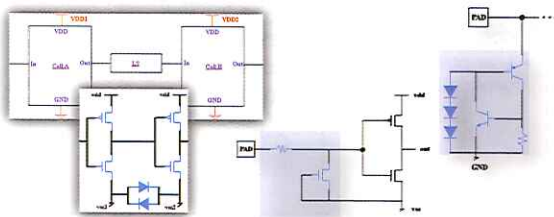
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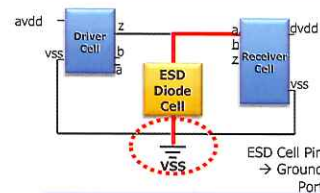
Solving Reliability Issues

Device and Cell Based Verifications

- Topological and Layout based checks
 - Reference cell names
 - Verify signals crossing multiple power domains
 - Addresses reliability concerns / EOS
- Layout centric verification with P2P, CD and DRC
 - Logic Driven Layout (LDL)
- User defined checks and feedback



Current density simulation



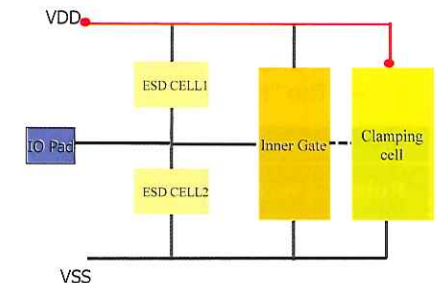
P2P resistance simulation

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Post-Layout Verification

P2P Parasitic Resistance Checking

- Increased wiring parasitic resistance affects the performance of circuit
- In real design, unexpected parasitic resistance in certain path can cause circuit malfunction



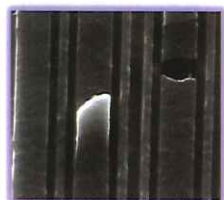
1. PERC topology checking to locate desired pin pair to measure effective resistance
2. PERC LDL to extract resistance network of nets where pin pairs resided
3. Compare against a constraint & report violations

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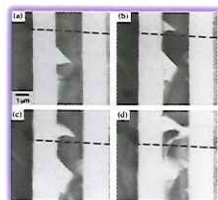
Post-Layout Verification

Current Density Checking (1/2)

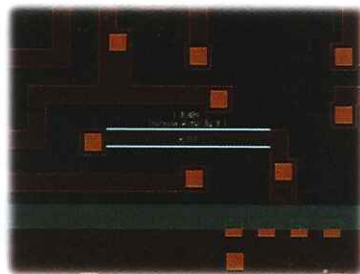
- High current density can cause opens or shorts in the design
- Therefore, there is a need to ensure robust current handling for the critical paths



Open



Short

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Post-Layout Verification

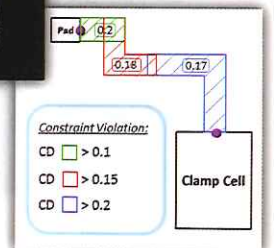
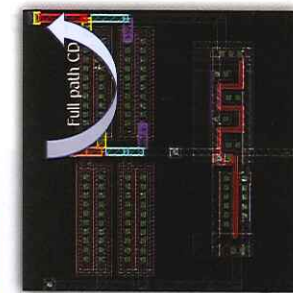
Current Density Checking (2/2)

Search for topology

Identify pins/ports of interest

Simulate current density for the relevant geometry

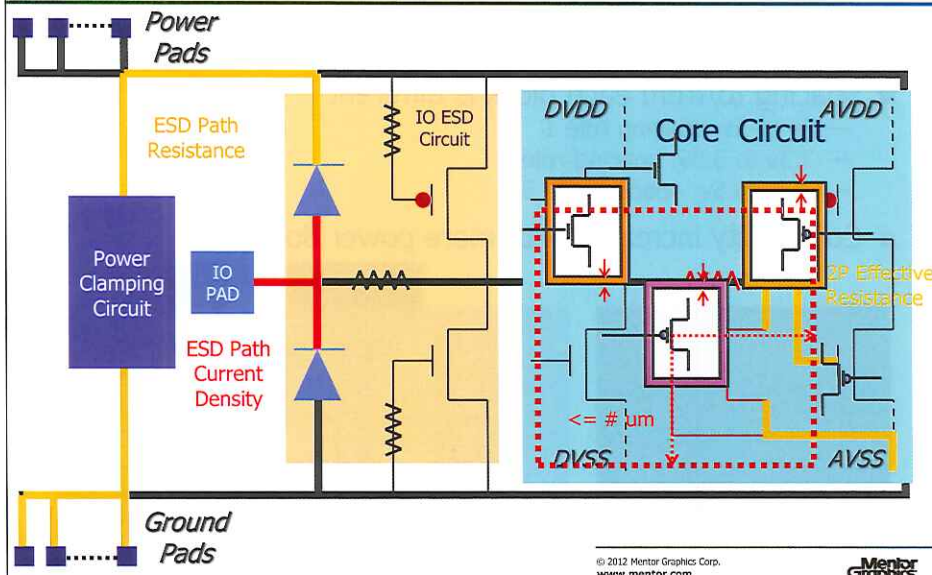
Compare against constraints & report violation



* CD units: mA/μm

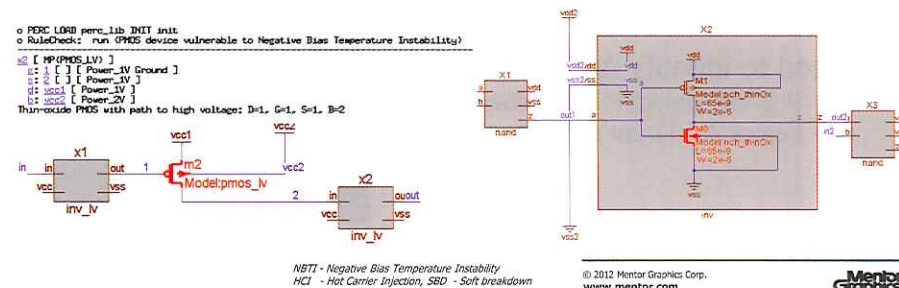
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Complete ESD / Latch-up Design Verification



Thin-oxide Gate Considerations for Overvoltage Susceptible to Reliability Issues (EOS)

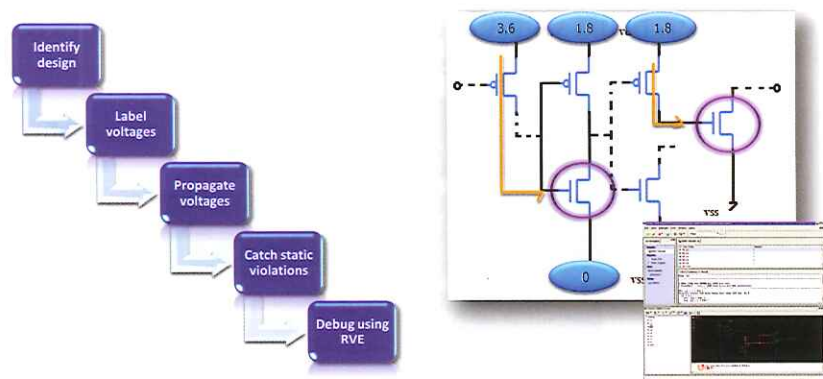
- Thinner-oxide → lower voltage → less power
 - Some power domain design errors lead to oxide breakdown and failure over time. NBTI (PMOS), HCI (NMOS), SBD
- Management of *bulk* and *power* pins in PnR environments
 - IP blocks may have internal global signals
 - Need to verify “gross” power domain crossing errors
 - Subtle design flaws may still require detailed simulation



Understanding EOS without Simulation

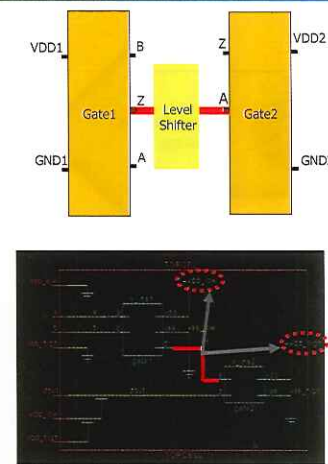
Voltage Propagation

- EOS has historically been one of the leading causes of integrated circuit failures, regardless of the semiconductor manufacturer
- The result of an EOS event can range from no damage or degradation to the IC up to catastrophic damage where the IC is permanently non-functional



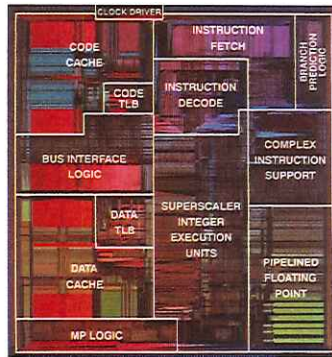
Power Domain Checking

- Low-power verification requires system knowledge and careful tracking of typically large numbers of domains
- One or more on and off chip power supplies.
 - Derived power supplies using Charge pumps, voltage dividers
 - Regulators/control blocks added to control the power to different blocks
 - Nonvolatile memories need more different voltage levels for different operations
 - Protection cells (i.e level shifters) between different power domains are critical for power management



Voltage Dependent DRC Checking

- Dies generally have multiple voltages
 - Voltage for specific region selected for best functional operation
- Difference in possible voltage values causes issues
 - Particularly true for automotive and other high power applications
- Some flows use marker layers
 - Try to avoid, can be error prone
- Need to identify Δv
 - Prevent dielectric breakdown
 - Larger Δv , larger spacing



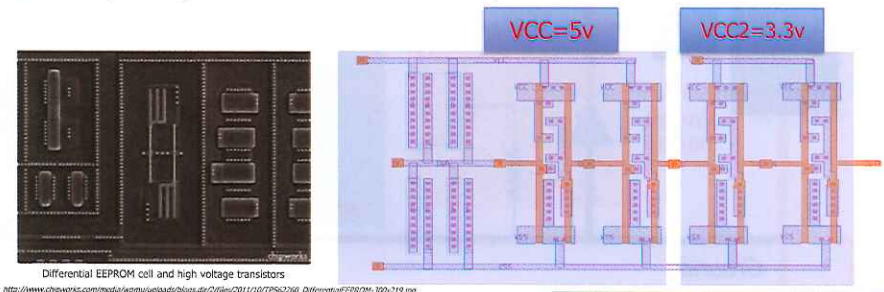
http://bmc.eecs.berkeley.edu/CICIda_photos/pentium.gif

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Voltage Dependent DRC Checking

- Different spacing checks required based on Δv
- Spacing to/from each block is different
 - 5v to 5v: spacing rule 1
 - 3.3v to 3.3v: spacing rule 2
 - 3.3v to 5v: spacing rule 3
- Complexity increases with more power domains

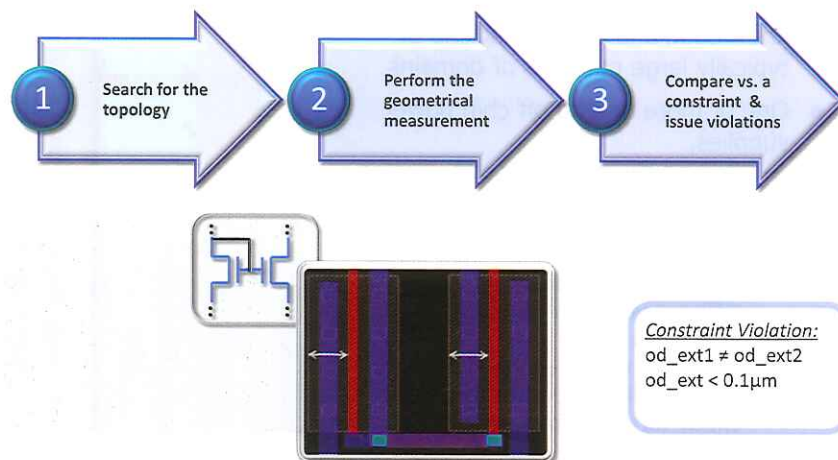


Differential EEPROM coil and high voltage transistors
http://www.chipworks.com/media/uploads/blogs/drc/2/files/2011/10/TPSG2260_DifferentialEEPROM_300-219.jpg

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Post-Layout Verification Topology-based Geometrical Checking

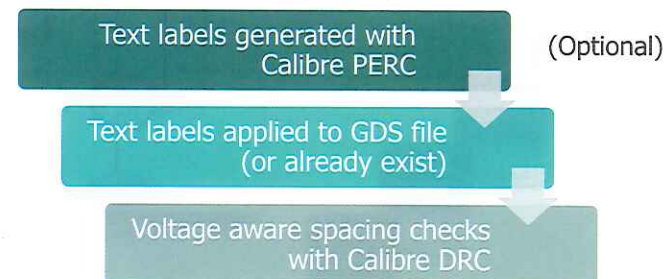


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Voltage Aware Spacing Checks Methodology in PERC

- Use existing text, or easily generate (Calibre PERC)
 - Flows without text are also possible with a Calibre PERC
- No complex marker layers
- Flow can begin with Calibre PERC, or directly with Calibre DRC (if texts already exist)

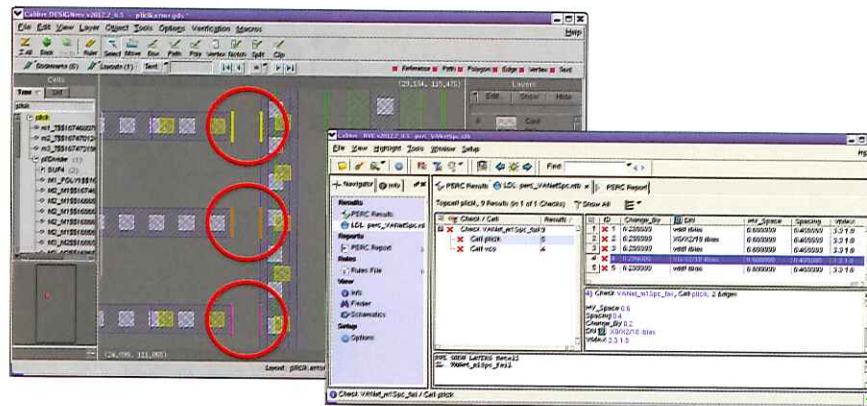


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Voltage Aware Spacing Checks Results Debug

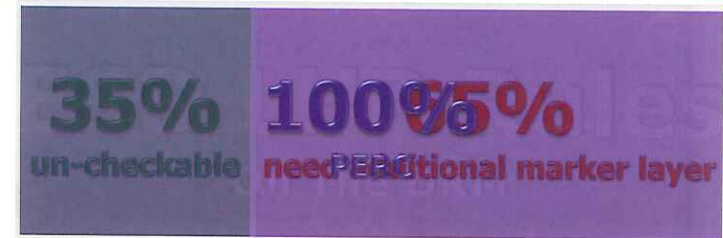
- Use existing text, or easily generate (Calibre PERC)
- No complex marker layers



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TSMC-Mentor Collaboration on Calibre PERC



- ESD/Latch-Up rules
 - Rules in the Design Rule Manual
 - 65% can be checked but tedious
 - 35% are unchecked
- MGC/Calibre collaboration delivers robust verification
 - No competitive offering
- Under Beta phase for deck quality enhancement

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Summary

- Calibre PERC continues to be a unique solution
 - Able to consider the specific context of the design
 - Verification Beyond "Traditional" DRC, LVS and ERC
 - Able to combine physical and logical aspects of your design
- Repeatable, efficient and effective reliability verification is needed to deliver solutions that meet our coverage requirements
 - Integrated and easy-to-use debug is a key aspect for an effective flow when deploying to end users
- Many customers adopting in wide range of process nodes and application spaces
 - For some, failure is not an option

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Automated Approach for Waiving Physical Verification Errors at IP

Mentor Graphics & LSI

ABSTRACT

Redundantly reviewing recurring errors Custom and third-party IP integration can slow down SoC verification. An automated waiver management methodology enables design and verification teams to specify and process a variety of design rule waivers, reducing debugging time and improving SoC results. This technology provides customizable control to waive errors only under certain conditions or constraints.



Automated Approach for Waiving Physical Verification Errors at IP

John Ferguson

Lead Technical Marketing Engineer, Calibre PV
Mentor Graphics Design to Silicon Division

Chuck Mayernik

Senior Engineer, Physical Verification, LSI Corporation

Jayanthi Pallinti

Senior Manager, MxS / PDK & Methodology, LSI Corporation

Chien-Ming Chiang

Senior Engineer, TSMC I/O Library Department



Agenda

- Why are waivers needed and what are the challenges?
- Introduction to Calibre Automatic Waivers
- TSMC inclusion of Calibre Automatic Waivers with 28nm IP Libraries

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Calibre Automatic Waivers Flow: LSI perspective

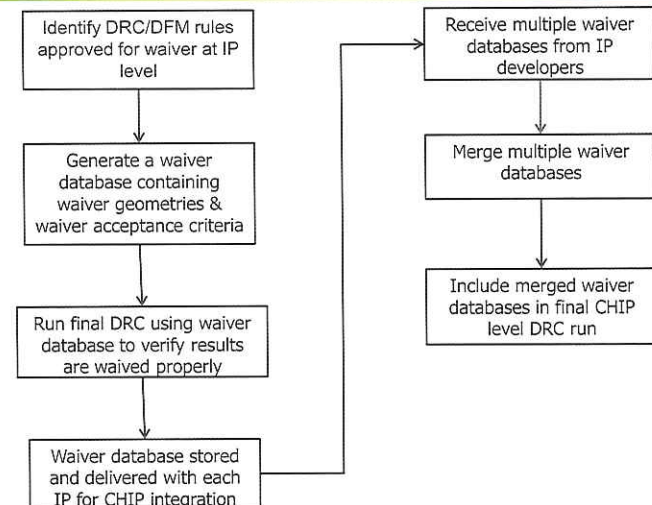
- Q: What is Waiver Flow?
- A: A formal hierarchical mechanism to identify and mask 'waived' IP-level DRC/DFM violations in a final chip level DRC run
- Why Calibre Automatic Waivers?
 - Advanced Technology Nodes have increased number of design rules
 - LSI design methodology uses recommended rule compliance wherever possible
 - Functional IP designed in early technology cycle can be still used 'as-is' when foundry updates design rule decks
 - Enables SoC designers to focus on correcting violations outside of IP
 - MGC Calibre Automatic Waivers flow allows waivers from IP to be carried to chip level
- LSI using MGC Calibre Automatic Waivers flow for 40nm and 28nm technologies currently and will continue at advanced technology nodes
 - Before waiver flow, manual review & waiver of approved DRC/DFM violations was done in redundant phases
 - Calibre Automatic Waivers increases efficiency for DRC sign-off at chip level

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Calibre Automatic Waivers Flow Current Usage



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Calibre Automatic Waivers: LSI Status & Challenges

Examples LSI Designs with Calibre Automatic Waivers							
Tech.	Design	Chip or IP	Waiver gds (MB)	Full chip/ IP (GB)	% Runtime change**	# IPs in Chip*	# IPs provided waiver gds
40nm	A	Chip	6.7	6.6	+15	16	9
	B	Chip	0.75	32	+23	60	29
28nm	D	Chip	1.3	35	- 18	83	71
	E	Chip	2.2	5.4	- 5	70	13

* Excludes memories & standard cells

** Increase or decrease in DRC runtime with waiver gds

- Current Status
 - At LSI, MGC Calibre Automatic Waivers is used for 40nm, 28nm technologies with plan to continue for advanced technology nodes
 - Number of IP blocks waived varies anywhere from 10 to 70
 - LSI has taped out 20+ 40nm designs & 5+ 28nm designs using Calibre Automatic Waivers
 - DRC runtime increase ~20% with waivers for 40nm; still justified since waivers are automated along with improved efficiency. 28nm runtimes decrease with waiver flow!
- Calibre Automatic Waivers Challenges
 - Implementation with standard cells is challenging due to abutment combinations
 - Coping with rule logic and name changes
 - Coping with different waiver criteria for the same rule
 - Run time performance

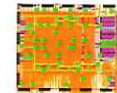
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Introducing Calibre Automatic Waivers

IP block containing errors to waive



Waivers merged with IP
by IP provider

Rules from foundry

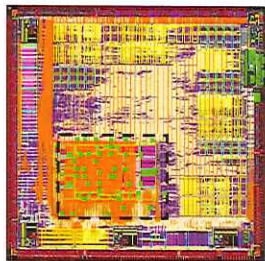


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Introducing Calibre Automatic Waivers



3rd party IP with waivers
embedded into design

Rules from foundry



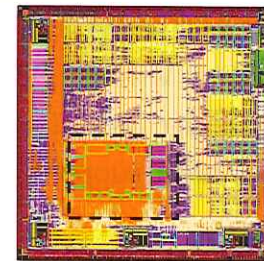
Waived results automatically removed at runtime

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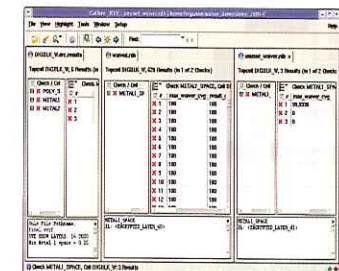
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Introducing Calibre Automatic Waivers



3rd party IP with waivers
embedded into design



Waived results saved for final review

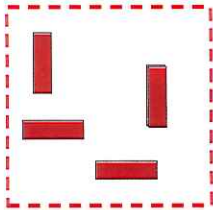
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Calibre Automatic Waivers Structure

Cell Nand2_2x



Waive\$wv\$_PO?\$46\$W?\$46\$R?\$46\$2_in_Nand2_2x

Waivers Saved in Layout

- GDSII, OASIS or Virtuoso DB
- Waiver subcell per waived rule
- Single waiver layer supports all rules

Additional Data in Text

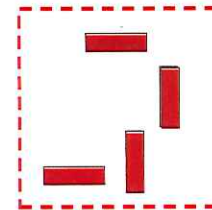
- Waiver criteria
- User name, date, comment
- Checksums to validate consistency

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Calibre Automatic Waivers Structure

Cell Nand2_2x



Waive\$wv\$_PO?\$46\$W?\$46\$S?\$46\$5_in_Nand2_2x

Waivers Saved in Layout

- GDSII, OASIS or Virtuoso DB
- Waiver subcell per waived rule
- Single waiver layer supports all rules

Additional Data in Text

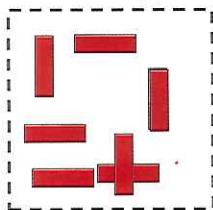
- Waiver criteria
- User name, date, comment
- Checksums to validate consistency

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Calibre Automatic Waivers Structure

Cell Nand2_2x



Waive\$wv\$_PO?\$46\$W?\$46\$R?\$46\$2_in_Nand2_2x

Waive\$wv\$_PO?\$46\$W?\$46\$S?\$46\$5_in_Nand2_2x

Waivers Saved in Layout

- GDSII, OASIS or Virtuoso DB
- Waiver subcell per waived rule
- Single waiver layer supports all rules

Additional Data in Text

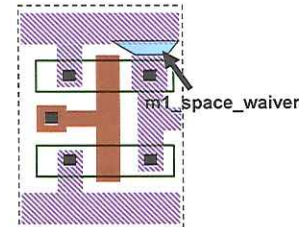
- Waiver criteria
- User name, date, comment
- Checksums to validate consistency

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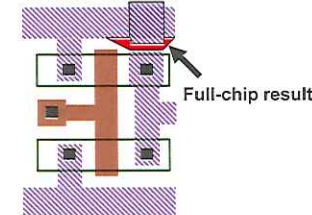
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Variable Waiving Shape Tolerance

Cell



Cell in Context



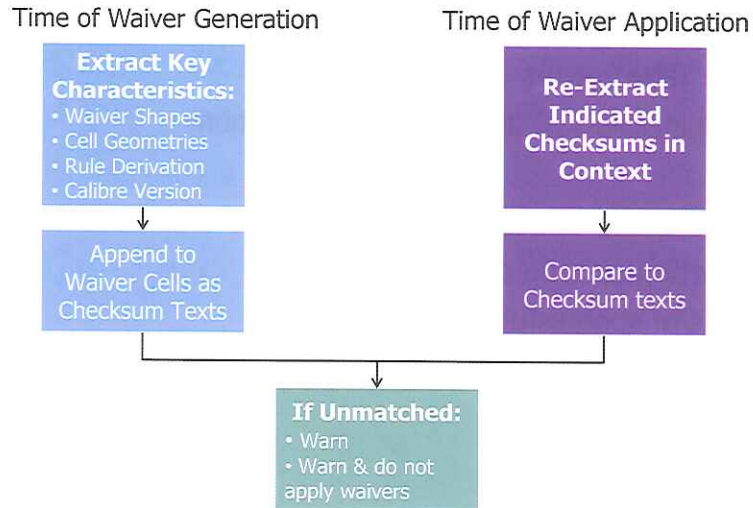
Waiver Criteria

- Specifies allowed shape distortion by percent area
- Specified per rule
- Set by file or save as text with the waivers

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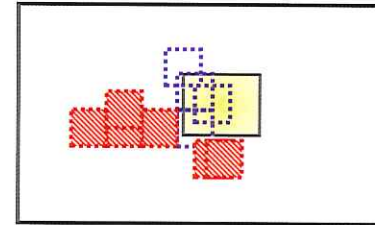
Validating Consistency and Integrity: Calibre Automatic Waivers Checksum Validation



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Special Handling for Non-Standard Rules



Support for more than just standard DRC violations

- Waive density results per window
- Traditional ERC and PERC rules
- Waiving in DFM/CFA with report cards
- Waive by Pattern Matching

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TSMC Waiving Needs for IP Deployment

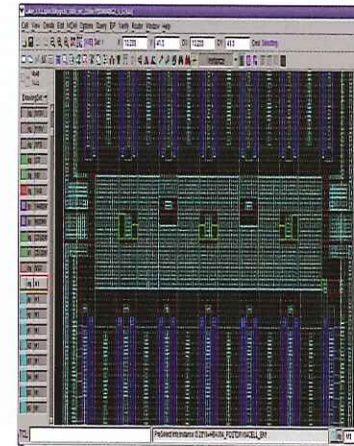
IP Provider Requirements

- No waiving of real errors
- No flagging of waived errors
- No dependency on hierarchy
- Access to majority of users
- Ability to easily incorporate and deliver with IP
- Cannot break competing PV tool flows

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TSMC Validation Process



Rigorous Testing of Calibre Automatic Waivers

- Waiver inclusion tested
 - DRC, LVS, DFM, PDK
 - Design flow & applications
- Tested across all tech-data
- Tested across IP
 - Stand alone and in context
- Validated Calibre's continued performance leadership

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TSMC Support for Calibre Automatic Waivers

Calibre Automatic Waivers in PDK

- Waiver layer and text layers reserved:
 - Layer 255
 - Datatypes 248-255

Calibre Automatic Waivers included with 28nm I/O Libraries

- Number of cells available with Calibre Automatic Waivers
 - >70 cells for DRC
 - >30 cells ERC
- Rules waived:
 - DRC 11
 - ERC 4

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Summary

Significantly Reduce PV Debug Times

- Remove "false" errors associated with IP
- Inclusion in TSMC IO libraries eases adoption

Safe and Trusted Waiver Methodology

- In production at > 35 companies
- Hundreds of successful tape-outs
- Accuracy and performance validated by TSMC at 28nm node

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This image shows a blank sheet of white paper with horizontal ruling lines. The lines are evenly spaced and run across the width of the page. There are no margins, text, or other markings on the paper.

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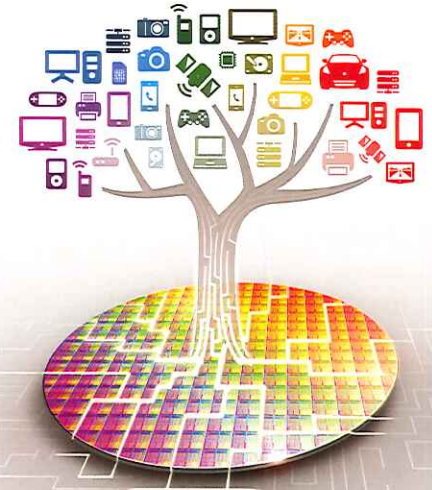
IP Track

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TSMC 2012 Open Innovation Platform® Ecosystem Forum

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TSMC IP Kit V2.0 – Enhancing Soft IP Quality Standards

Atrenta



ABSTRACT

TSMC and Atrenta launched the soft IP qualification program in 2011. Since that time, 13 IP partners have joined the program to date. In this presentation we will discuss the TSMC IP Kit, which is a joint development between TSMC and Atrenta using the SpyGlass platform for IP handoff analysis and validation. We will review the tests that are part of the Kit, show example quality metrics and DataSheet reports, and discuss the kind of design issues that have been uncovered and fixed as a result of the program. We will also discuss the new version of the IP Kit (TSMC IP Kit 2.0) that is under joint development between TSMC and Atrenta. This version of the Kit adds physical analysis of the IP (e.g., routing congestion) as well as advanced formal metrics that explore the complexity and ease of verification for the IP. We will present the timeline for implementation of IP Kit 2.0 and the results of our testing of IP Kit V2.0 with IP partners.





TSMC IP Kit V2.0 – Enhancing Soft IP Quality Standards

Anuj Kumar
October 2012

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Short History – TSMC/Atrenta Program



- TSMC and Atrenta announced a Soft IP Qualification Flow in May 2011

Atrenta Announces SpyGlass Tool Used In TSMC Soft IP Qualification Flow

Quality reports generated by SpyGlass® to be available on TSMC web site

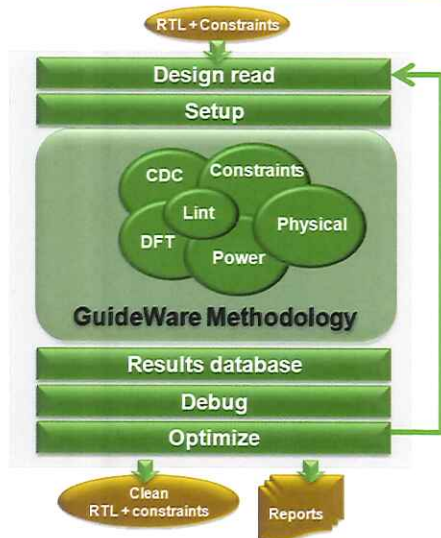
San Jose, Calif. and HSINCHU, Taiwan, R.O.C. — May 26, 2011 — Atrenta Inc. today announced the deployment of a comprehensive soft IP qualification program using Atrenta's SpyGlass® platform and a targeted subset of its GuideWare reference methodology in TSMC's IP quality assessment program. The goal of the program is to provide quantitative information to TSMC's customers regarding the robustness and completeness of synthesizable semiconductor IP that is part of the TSMC 9000 IP library. All the software and methodologies needed to implement TSMC's IP qualification requirements have been integrated by Atrenta to form the IP Handoff Package.

- Focus – qualify the robustness and completeness of synthesizable IP that is part of the TSMC 9000 library for TSMC's customers
- Summary of flow & partner momentum...

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Key Component – SpyGlass

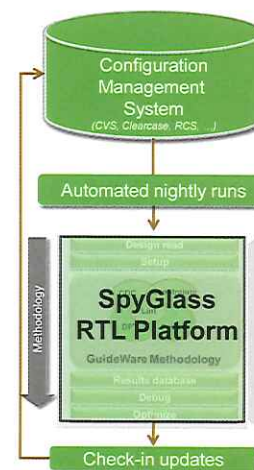


- Complete platform to optimize RTL - Lint, CDC, DFT, Constraints, Power and Routing Congestion
- GuideWare provides best practices for high impact, low noise analysis
- RTL problems easily identified
- Richest set of engines that identify real implementation issues

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SpyGlass Data Management Addition



Automatically generates
HTML DashBoard and DataSheet reports
to track design quality & design specs



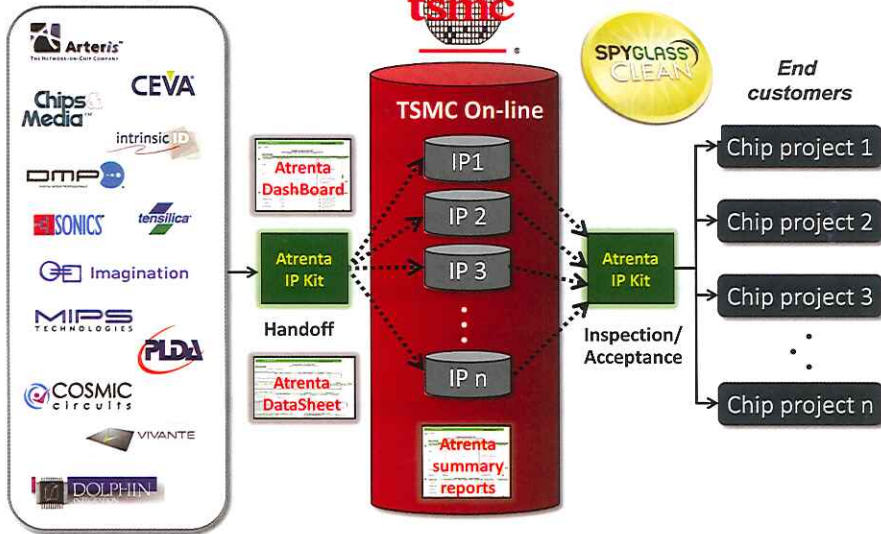
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Program Overview



IP ecosystem partners



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WHAT DOES TSMC IP KIT 2.0 CHECK AND WHAT HAVE WE FOUND?

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Sample Tests – IP Handoff Kit V 1.0



- Power**
 - What will the average power dissipation be?
 - Are my power domains correctly defined?
- Clocks & Timing**
 - Are clock and reset constraints set properly?
 - Are clock definitions consistent, correct and complete?
 - Are clock domain crossing synchronizers bug-free?
 - Are timing constraints consistent across block boundaries?
 - Are false path and multi-cycle paths correctly identified?
- Lint**
 - Is the design ready for simulation and synthesis?
- Test**
 - What will the stuck-at and at-speed test coverage be?
 - Can all sequential elements be scanned?

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What Did We Find?



Many items that would impact integration/debug time and chip function were found & fixed

Some examples:

- Missing synchronizers on CDC paths causing possible chip function issues
- Data loss on a fast-slow CDC paths
- Uncontrolled data path impacting transition fault coverage
- Index out of range which causes synthesizability issues
- Unconstrained I/O ports leading to poor SDC coverage

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IP Kit 2.0 – Need & Motivation



■ Improve soft IP handoff quality checks

- Align TSMC IP Kit methodology with Atrenta's latest GuideWare 2.0 methodology providing high coverage and low noise IP handoff checks
- Introduce additional design checks
 - Advanced formal lint (e.g., X-assignment, dead code detection, etc.)
 - Physical implementation data (e.g., area, timing & congestion)

■ Improve the IP Kit setup & flow execution

- Automatic generation of setup files
- Flexibility in goal running (single/multiple/goal group)
- Incremental analysis

■ Easier integration of SpyGlass in customer's existing design flow

■ Improved IP packaging

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IP Kit 2.0 – TSMC/Atrenta Collaboration



■ Golden Rules for soft IP handoff analysis

■ Definition of quality metrics to assess soft IP

- Modified severity of errors to conform to quality requirements

■ Enable various IP packaging types

■ Optimize work flow to ensure ease-of-use and reliable, fast operation

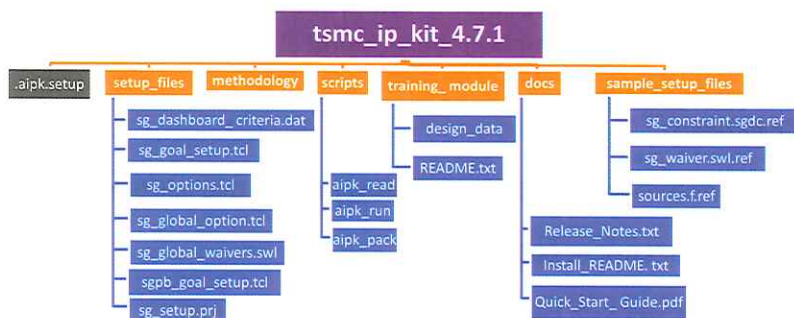
- Tuned mandatory vs. optional goals

■ Joint roll out plan development and beta testing with IP partners

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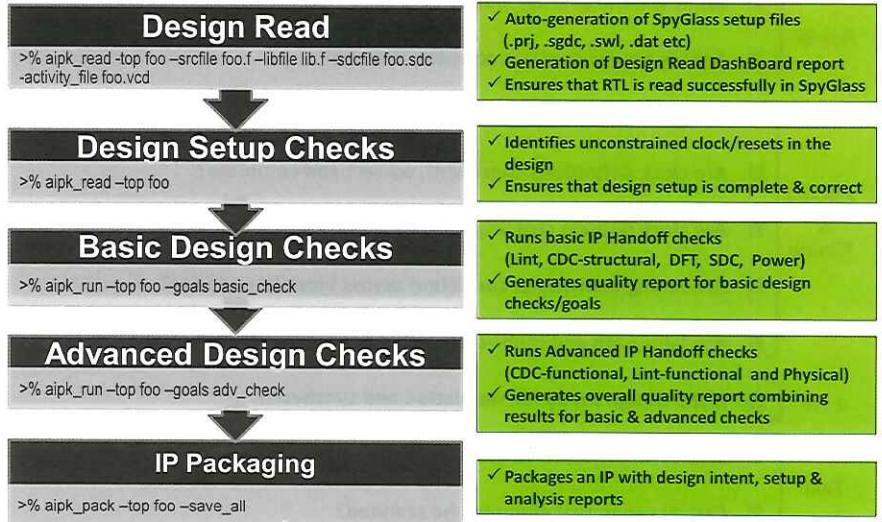
TSMC IP Kit 2.0 Package Structure



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TSMC IP Kit 2.0 Execution Flow



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Design Read DashBoard Report



ATRENTA

DashBoard

SpyGlass Report for ip_top
Created: Sat Mar 31 20:51:49 IST 2012 by anujk

Expand All >>>

Show Passed Items
Show Failed Items

ip_top					
Design Objectives	Run Status	Value	Graph	Success Criteria	Pass/Fail Status
DesignRead	Completed	BlackBoxes Errors = 0		BlackBoxes Errors = 0	✓
	Completed	GreyBoxes Errors = 0		GreyBoxes Errors = 0	✓
	Completed	Elaboration Errors = 0		Elaboration Errors = 0	✓
	Completed	Synthesis Errors = 0		Synthesis Errors = 0	✓
	Completed	Tech Lib Cells Used = 0		Tech Lib Cells Used = 0	✓
CDC_Setup	Completed	Unconstrained Clocks = 0		Unconstrained Clocks = 0	✓
	Completed	Unconstrained Resets = 0		Unconstrained Resets = 0	✓
SDC_Setup	Completed	SDC Errors = 2		SDC Errors = 0	✗
	Completed	Missing Clocks Constraints in SDC = 0		Missing Clocks Constraints in SDC = 0	✓
	Not started	Missing IO Constraints in SDC = NA		Missing IO Constraints in SDC = 0	⚠
Summary	Not completed			Failed objectives = 1	✗

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TSMC IP Kit 2.0 – Mandatory Goals



Domain	Goal Name	Purpose	Handoff Check Type
Lint	lint_rtl	Checks the design for simulation/synthesis readiness, connectivity & structural issues	Basic
	clock_reset_integrity	Checks the integrity of clock and reset propagation and architecture	Basic
Advanced Lint	adv_lint_struct	Checks for X-assignment, FSM transition, deadlock issues based design topology analysis	Advanced
	adv_lint_verify	Checks the functional issues in FSM transition, static code, bus overflow & X-assignments based on formal verification analysis	Advanced
CDC	cdc_setup_check	Checks the completeness of clock & reset constraints	Basic
	cdc_structural_check	Exhaustive verification all synchronization checking for CDCs and asynchronous reset signals based on design topology checking	Basic
	cdc_functional_check	Exhaustive verification of functional aspects of the CDC path and synchronizers using formal analysis techniques	Advanced
DFT	dft_best_practices	Checks the design for best practices to increase ATPG effectiveness and efficiency	Basic
	dft_scan_ready	Checks if all sequential elements are scannable or not. Also generates the coverage audit report	Basic
	dft_test_points	Helps in improving the test coverage by identifying the uncontrollable and unobservable nodes in the design	Basic
	dft_dsm_clocks	Helps in defining the clocks used for at-speed testing and any associated PLL, etc.	Basic
	dft_dsm_best_practices	Addresses special needs of cases such as d-pin controllability, test clock domains and path issues. Also generates the transition coverage audit report	Basic

Legend: Goal Enhanced New Goal Added

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TSMC IP Kit 2.0 – Mandatory Goals



Domain	Goal Name	Purpose	Handoff Check Type
Power	power_est_average	Estimates the average power of the design	Basic
Power Verification	power_verif_instr_rtl	Verifies the desired power intent in the RTL design as per given power constraints	Basic
Constraints	sdm_setup_check	Performs sanity checking on SDC file	Basic
	sdm_audit	Computes constraints coverage for design objects like as IOs, flops, etc.	Basic
	sdm_check	Ensures that clock & IO delay definitions defined in the SDC file are consistent, correct & complete	Basic
	sdm_exception_struct	Ensures that given timing exceptions constraints exist in the design	Basic
	sdm_redundancy_check	Help in removing the redundancy in constraints definition	Basic
TXV	fp_verification	Helps in the verification of false path constraints	Advanced
	mcp_verification	Helps in the verification of multi-cycle path constraints	Advanced
Physical	physical_analysis_signoff	Performs physical analysis using vendor library, used for signoff on area, congestion and timing (based on pre-floorplan checks)	Advanced

Legend: Goal Enhanced New Goal Added

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TSMC IP Kit 2.0 – Optional Goals



Domain	Goal Name	Purpose	Handoff Check Type
Lint	design_audit	Provides basic design profile data and generates the IO data for the population of DataSheet reports. This goal is automatically run during IP Kit Design Read stage, hence kept as an optional goal and user does not need to run it explicitly	Basic
Power	power_audit	Reports all given key design data, inputs and parameters, which will be used for power estimation analysis. This report indicates the completeness of design setup for power estimation analysis. This goal is automatically run during the IP Kit Design Read stage, hence kept as an optional goal and user does not need to run it explicitly	Basic
	power_est_cycle	Calculate power for each cycle of the simulation profile file. As this goal computes power for each cycle of simulation waveform, it may take huge run time if given simulation file(VCD/FSD) is quite big, hence kept as an optional goal	Basic
Power Verification	power_verif_audit	Does the audit/completeness check on given UPF/CPF file. This goal is automatically run during the IP Kit Design Read stage if the user has provided any power intent file like UPF or CPF, Hence kept as an optional goal	Basic
Constraints	sdm_hierarchical_check	Ensures that constraints are consistent across the block boundaries. This goal would become applicable for running if SDC files exist both for the top design and underlying sub-blocks	Basic
	sdm_equiv	Ensures that different versions of the SDC files are equivalent for the same design. This goal can only be run if there exist two sets of the SDC file(s) for an IP	Advanced
Physical	physical_library_preparation	Prepare the technology library in the requisite OA format, which is a must for running other SpyGlass Physical goal runs. This goal is automatically run during the IP Kit Design Read stage, hence kept as an optional goal and user does not need to run it again explicitly	Advanced

Legend: Goal Enhanced New Goal Added

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TSMC IP Kit 2.0 vs. 1.0 Benchmark Data



Design Quality Objective	IP#1		IP#2		IP#3		Comments
	IPK 2.0	IPK 1.0	IPK 2.0	IPK 1.0	IPK 2.0	IPK 1.0	
Unsynchronized CDC paths	236	240	0	0	102	106	CDC goal optimized to avoid false unsynchronized violations
Stuck-at fault coverage	82.7	82.7	100	100	99.8	99.8	
Stuck-at test coverage	83.7	83.7	100	100	99.8	99.8	
% of scannable flops	89	89	100	100	99	99	
Transition fault coverage	51.3	51.3	95.5	95.5	73.3	73.3	
Transition test coverage	77.7	77.7	95.8	95.8	95.2	95.2	
% of IO ports constrained in SDC file	99.9	99.9	100	100	100	100	
% of registers constraints in SDC file	100	100	100	100	100	100	
Switching power(in mW)	0.32	0.32	5.98	5.98	2.24	2.24	
Internal power(in mW)	1.05	1.05	44.2	44.2	11.5	11.5	
Leakage power(in mW)	0.005	0.005	0.13	0.13	0.02	0.02	
Total power(in mW)	1.37	1.37	50.3	50.3	13.8	13.8	

Legend:

Improved QA

Additional QA

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Benchmark Data (cont'd)



Design Quality Objective	IP#1		IP#2		IP#3		Comments
	IPK 2.0	IPK 1.0	IPK 2.0	IPK 1.0	IPK 2.0	IPK 1.0	
Gate count (NAND equivalent)	9.2K	9.9K	1.72M	2.2M	48K	70.5K	Gate count calculation is more accurate in IP Kit K2.0 – based on SpyGlass Physical analysis
Flop count	741	745	50422	53581	4490	4546	
Latch count	5	5	1175	1179	0	0	
No. of timing paths failing	0	NA	0	NA	0	NA	
No. of congested module instances	0	NA	10	NA	0	NA	
Floating inputs	0	0	0	0	0	0	
Multiply driven nets	0	0	0	0	0	0	
Cyclomatic complexity	63	NA	1559	NA	257	NA	
Run time for common (existing) goals	824	1109	8197	9520	9550	9616	Run time reduced an average by 10-15% for common goals
Total number of errors	619	386	1147	125	122	115	New & improved error rules catching additional critical design issues
Total number of warnings	796	1369	1911	7614	214	918	Goal enhancement/optimization helped to control the violation reported for less severe rules (warnings)

Legend:

Improved QA

Additional QA

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IP Specification Report



The TSMC IP Kit generates the SpyGlass DataSheet report capturing key design specifications and profile statistics, once all goals run are finished

ATRENTA

DataSetSheet

IO Definitions (13 ports) [Collapse](#)

Pin	Dir	Range	Type	Ref Clock	Reg	Synch	IO Delay ^(c)	Mode ^(c)	Description
ahbmi	INPUT	[87:0]	-	clk	Yes	-			-
		[0:14]	-						
		[15:50]	clk						

Clock Trees (2 clocks) [Collapse](#)

Clock	Mode	Freq	Domain	# Domain Crossings	Posedge				Total	Negedge				Total	Source
					Reg	Latch	Lib cell	Black Box		Reg	Latch	Lib cell	Black Box		
clk	sys-clock	200 MHz	d2	0	454	0	0	0	454	0	0	0	0	0	SDC/SGDC
pciclk	sys-clock	500 MHz	d1	0	358	0	0	0	358	0	0	0	0	0	SDC/SGDC

Design Physical Profile [Collapse](#)

Logic Type	Instance Count	Gate Count	Area	Area %age
Synthesizable gates	20505	92274	0.063 mm ²	63%
Memories	105	39546	0.027 mm ²	27%
Hard Macros	5	14646	0.010 mm ²	10%
Blackboxes	0	0	0.0000 mm ²	0%
Total	20615	146466	0.1 mm ²	100%

Timing [Collapse](#)

Clock	Period	Number of Failing Paths	Maximum Logic Levels
pcidma_pciclk	2.000 ns	0	11
pcidma_clk	5.000 ns	0	19
FEDERER	5.000 ns	-	-

Congestion [Collapse](#)

Module Name	Hierarchical Instance Name	Standard Cell Count	Internal Congestion Score	Peripheral Congestion
** No congested module found **				

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Design Quality & Status Summary Report



The TSMC IP Kit generates a SpyGlass DashBoard report capturing the high-level design quality metrics and goal run summary report, once all goals run are finished

ATRENTA DashBoard									
pcidma									
Design Objectives	Run Status	Value	Graph	Success Criteria	Pass/Fail Status				
CDC	Completed	Unsynchronized crossings = 26		Unsynchronized crossings = 0	✗				
	Completed	Synchronization coverage = 61% (42/68)		Synchronization coverage = 100	✗				
	Completed	Failed properties = 41% (15/36)		Failed properties = 0%	✗				
	Completed	Stuck at fault coverage = 92.4		Stuck at fault coverage > 90	✓				
DFT	Completed	Stuck at test coverage = 98.1		Stuck at test coverage > 98	✓				
	Completed	Percentage of scannable flops = 100.0		Percentage of scannable flops > 100	✗				
	Completed	Transition fault coverage = 76.4		Transition fault coverage > 90	✗				
	Completed	Transition test coverage = 94.0		Transition test coverage > 98	✗				
Constraints	Completed	Percentage of ports constrained = 99.78		Percentage of ports constrained = 100	✗				
	Completed	Percentage of registers constrained = 100.00		Percentage of registers constrained = 100	✓				
Power	Completed	Switching Power = 2.22mW		Not set					
	Completed	Internal Power = 4.14mW		Not set					
	Completed	Leakage Power = 66.8uW		Not set					
	Completed	Total Power = 6.43mW		Not set					
Quality Goals	Run Status	Unresolved Messages			Waived Messages			Graph	Pass/Fail Status
		FATAL	ERROR	WARNING	ERROR	WARNING			
lint_ni	Completed	0	12	64	0	0		Fatal =0, Error =0	✗
design_audit	Completed	0	0	3	0	0		Fatal =0, Error =0	✓

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Summary – TSMC IP Kit 2.0 vs. 1.0



Ease-of-Use:

- Easier to install: No need to copy 'spyglass' package each time for each new IP
- Short learning curve: Common use model for new SpyGlass Physical Base goals

Improved IP Handoff Methodology:

- Added new goal checks(Advanced Lint & SpyGlass Physical Base) covering additional design checks/analysis
- Improved/optimized the existing goals to provide high coverage & low noise
- Noise reduction by removing 'Power Reduction' goal, which is not applicable for IP handoff checking

Improved Flow & Reports:

- Provides a lot more flexibility and guidance while executing IP Kit 2.0 flow
- Design analysis divided in 2 steps(basic_check & adv_check) for efficient, systematic and meaningful analysis of the design on all recommended design goals
- DashBoard report now shows additional design parameters
- Multiple goal run reports for detailed review/analysis of easily accessible
- Improved IP packaging



Thank you!

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1T-OTP – Non-Volatile Memory for Mobile and Other Low-Power Applications

Sidense

ABSTRACT

Mobile devices such as smartphones are driving significant growth in the semiconductor industry. Manufacturers continue to introduce evermore complex devices, pushing the development of new technologies. More system complexity is moving on-chip and device manufacturers are faced with more challenges to maximize battery life while adding more features and pushing the performance envelope.

Embedded non-volatile memory (NVM) and, in particular, one-time programmable (OTP) memory, is used in an increasing range of ICs used in mobile devices. The intrinsic process-node portability and scalability of one-transistor (1T) antifuse-based OTP memory allows TSMC's customers to choose between several process variants over various process nodes. This helps them optimize for requirements such as longer battery life, lower system cost and higher performance. With TSMC's well-established IP partners program and its IP9000 Assessment program for establishing high levels of consistency, completeness and quality by its IP partners, the TSMC-Sidense partnership helps assure our common customers that the 1T-OTP IP they license from Sidense will meet their quality and reliability objectives.

This presentation will cover the following topics:

- A brief overview of non-volatile memory, its current uses and emerging applications in power-sensitive applications such as mobile devices.
- The key requirements for devices used in mobile applications and their considerations when investigating suitable NVM solutions. These requirements include performance, cost and data security and, as battery life is critical, managing power and minimizing power consumption.
- An overview of 1T-OTP and its features including low power consumption, field programmability, high security and high density that make it a preferred alternative over other types of NVM for mobile applications.
- An exploration of 1T-OTP features along with methods for minimizing power in mobile devices.
- Examples of 1T-OTP implemented in a wide range of TSMC processes and in various power-sensitive applications including PMICs, media processors, sensors, camera modules and timing devices.

The presentation will show how the complexity of mobile consumer devices, coupled with the need for power-efficient, cost-effective, reliable and secure storage, is met using 1T-OTP. The ability of Sidense 1T antifuse OTP to seamlessly fit into a broad range of TSMC processes lets our common customers benefit from the combination of TSMC foundry and IP services and Sidense's 1T-OTP NVM solution.



1T-OTP – Non-Volatile Memory for Mobile and Other Low-Power Applications

Craig Downing – Product Marketing Manager, Sidense

TSMC Open Innovation Platform

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Agenda

- Non-Volatile Memory
- Mobile and other low-power device requirements
- 1T-OTP Overview
- 1T-OTP solutions for low-power applications
- Summary

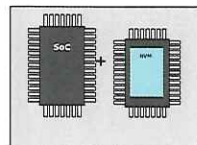


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The Future of Logic NVM™

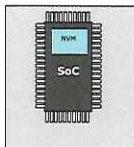
Non-Volatile Memory

Discrete NVM Devices



	Technology
Flash	Floating gate. Block erase
EEPROM/PROM	Floating gate.

NVM Embedded on Chip



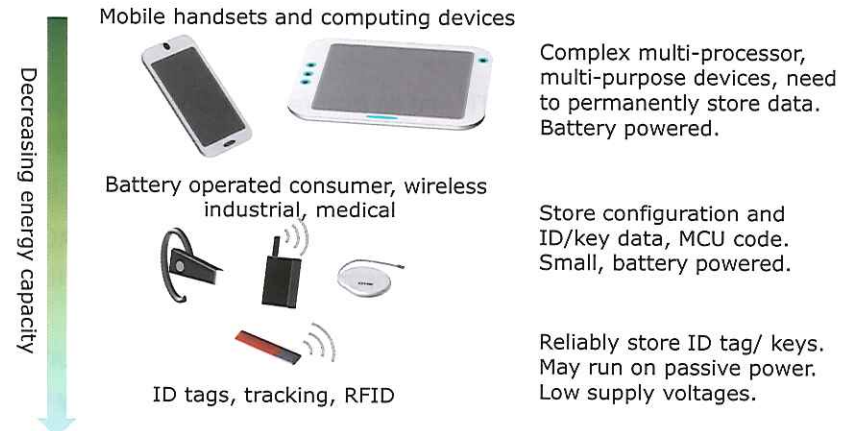
	Technology
Antifuse OTP	Permanent oxide breakdown, on-chip programming
Fuse/eFuse	Polyfuse/ metal fuse blowing
Mask ROM	ROM pattern fabricated on chip
Flash/MTP	Floating gate. On-chip erase/program



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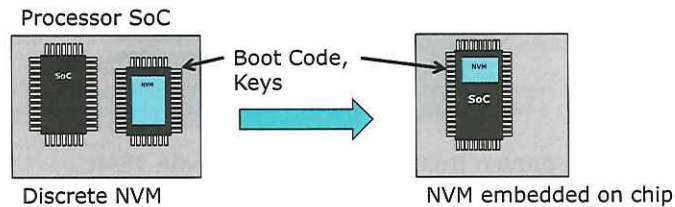
Mobile and other low power applications



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The Future of Logic NVM™

Embedding NVM Better Meets Most Requirements



- Smaller footprint
- Lower Cost
- Lower Power
- More Secure
- More Reliable
- Faster start-up (Execute code in place)



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The Future of Logic NVM™

Mobile Handset NVM Requirement



- Minimize Cost
- Maximize Battery Life
- Pack in More and More features
- Data Security (more IP, sensitive data)

	Boot Code	Encryption Key/ ID	Trim/ Calibration	Mass Media File storage
App/Media Processor	•	•	•	•
Baseband	•	•		
Camera	•			
Display Controller	•		•	
RF/Power/Analog			•	
Connectivity	•	•	•	
PMIC	•		•	
Sensors			•	

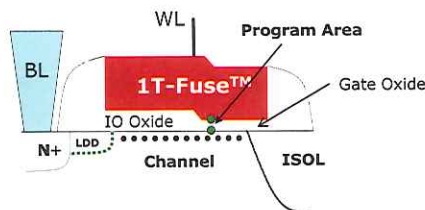
Program once/few times => OTP



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The Future of Logic NVM™

Antifuse: Sidense 1T-OTP Bit Cell (1T-Fuse™)



- Patented 1T Split-Channel OTP architecture
- Reliably programmed through a controlled, non-reversible oxide breakdown
- Breakdown is from gate-to-channel only

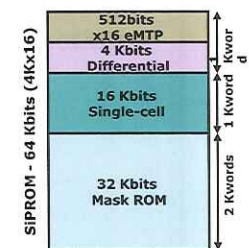
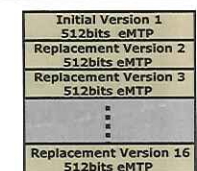


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The Future of Logic NVM™

1T-OTP Field Programmability: eMTP Operation

- Emulate Multi-Time-Programming for: Code revisions, encryption key updates in-field.
- Small footprint permits reserving OTP space for data to update in field.
- Simple write operation to update compared to erase/write procedure in traditional NVM (e.g. Flash) – Single bit write.
- Single Macro can support multiple uses: eMTP, fixed ROM, different read modes.

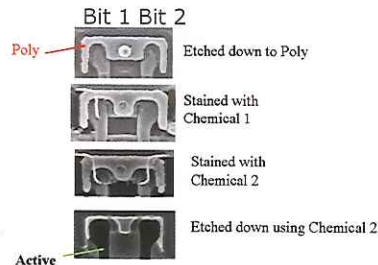


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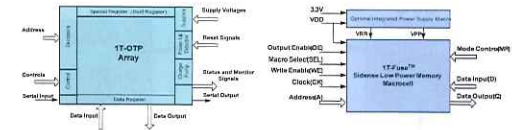
The Future of Logic NVM™

1T-OTP: Highly Secure NVM

- Secure key, code and data storage for applications including mobile SoCs.
- 1T-OTP bit-cell is very difficult to reverse engineer: No visible difference between programmed and un-programmed bit.
- 1T-OTP macros incorporate other features for additional security, including a differential read mode (no power signature).



Sidense 1T-OTP Macros



- Silicon proven from 180nm to 28nm with TSMC.
- No extra masks or processing steps.
- Many 1T-OTP products have met TSMC IP-9000 Assessment Criteria with others in progress.
- Small footprints, High densities:
 - Minimal impact on die area and cost.
 - Power-efficient
- Very secure and reliable.
- Read mode options support lower voltage operation.
- Field programmability. Easy ROM conversion.



Sidense & TSMC Collaboration

- Process node support from 180nm to 28nm.
- Different process variants supported including BCD.
- Working with TSMC, many Sidense 1T-OTP products have already met IP-9000 Assessment criteria. Others in progress.
- 1T-OTP products are available at various TSMC fab locations. We are working together to qualify more.



1T-OTP for 130nm to 40nm SiPROM

TSMC Process Support:
130nm to 40nm

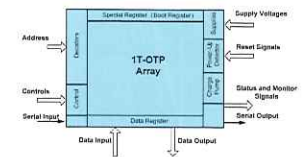
Uses: Secure Code and Key Storage. ROM replacement

Typical Applications:

Media Processors, HDTV encryption,
Network processors, Peripheral
Controllers, Wireless and Interconnect.

Features:

- High Densities (up to 512Kbits per macro)
- Small footprint
- Low Active and Standby Power
- Field Programmable
- Multiple read modes



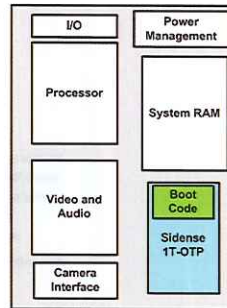
Mobile SoC example TSMC 65nm LP

Boot code stored on-die using 1T-OTP

- Code executes from OTP
- Support field updates (emulate MTP)
- Secure macro protects IP

Multiple uses for 1T-OTP macro:

- Small footprint, cost and power efficient.
- Secure encryption key storage
- Configuration data.



Media Processor with
Sidense SiPROM OTP
TSMC 65nm LP



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The Future of Logic NVM™

Very Low Power Applications

Decreasing energy capacity

Battery operated consumer, wireless
industrial, medical



Store configuration and
ID/key data, MCU code.
Small, battery powered.

ID tags, tracking, RFID

Reliably store ID tag/ keys.
May run on passive power.
Low supply voltages.



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The Future of Logic NVM™

180/152nm G, BCD SLP – Very Low Power NVM

TSMC Process Support:

180/152nm G 3.3V – IP-9000 Assessed
(multiple TSMC fabs supported).
180nm BCD, G 5V (Automotive 150°C).

Uses:

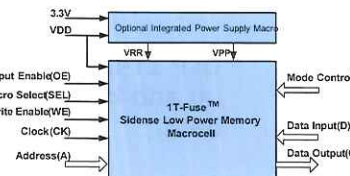
Trim/Calibration, Code and Key Storage.

Typical Applications:

Mobile, automotive, MCU, sensors, analog,
audio, timing/clocks.

Features:

- Designed for low-power operation and standby.
- Small footprint.
- Field Programmable.
- Multiple read modes.



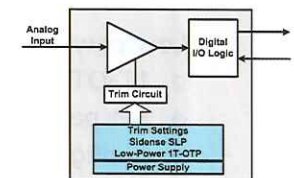
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The Future of Logic NVM™

Example – Trimming Analog ICs

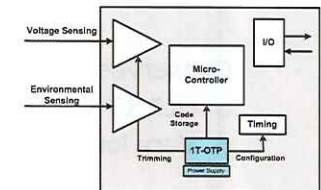
Analog trimming example – Sensor IC

- 1T-OTP stores trim settings
- Output bits drive trim circuit



Support multiple uses - PMIC example

- Analog Trim
- Code storage
- Configuration



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The Future of Logic NVM™

180nm G ULP– Ultra Low Power NVM

TSMC Process Support:
180/152nm G 3.3V – IP-9000 Assessed
(multiple TSMC fabs supported)

Uses:

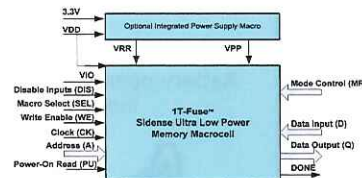
Trim/Calibration, Configuration

Typical Applications:

Sensors, analog, timing/clocks, RFID

Features:

- Designed for very low power operation
- Low voltage power on read mode to minimize system power.
- Small footprint
- Field Programmable
- Optional integrated power supply and charge pump

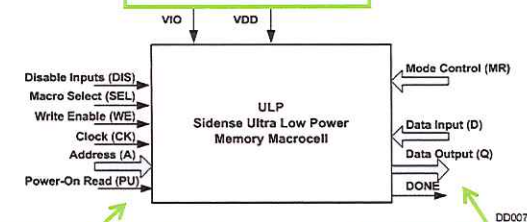


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The Future of Logic NVM™

ULP: Very Low Power Operation Low Voltage Read

Read Operation with:
 $VIO \ll VDD$
 $VDD < 1.8V$



Set Power-On Read:
One-shot read of Word

Once data latched VDD
can be removed to
further save power. Only
need VIO.



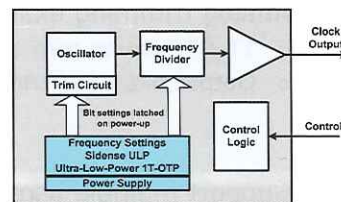
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Example – Timing device

Low power timing IC

- 1T-OTP stores trim settings
- Set parameters at test
- Configure product specs.
- Field programmable



Conserves system power

- ULP 1T-OTP macro loads setting on power-up
- Very low power standby operation



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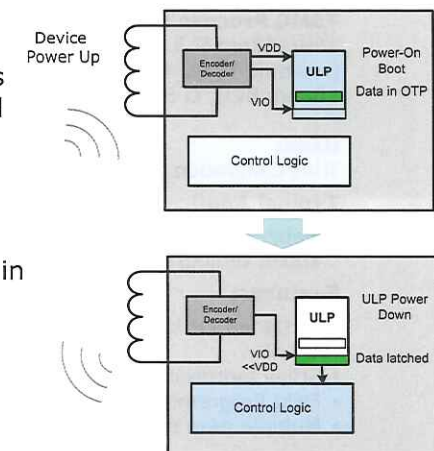
The Future of Logic NVM™

RFID Example

ULP 1T-OTP macro powers up and loads programmed data.

ULP consumes nanowatts in low-power mode.

Conserving energy while device responds.



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The Future of Logic NVM™

Summary

- 1T-OTP is an ideal solution for low power applications.
 - Best fit with evolving NVM requirements in mobile.
 - Enables very low power applications
- Broad TSMC process support 180nm to 28nm
- Assessed for TSMC IP-9000 across many nodes and process variants

info@sidense.com

www.Sidense.com

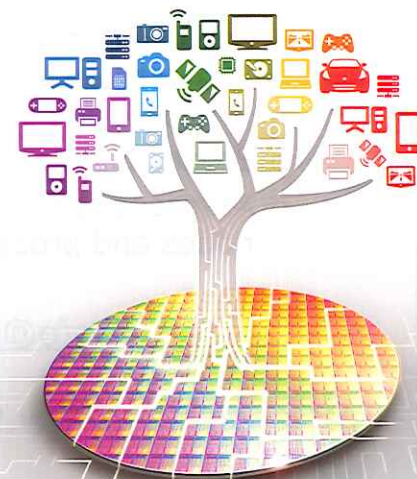


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The Future of Logic NVM™

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Implementing and Optimising Graphics IP in SoCs

Imagination Technologies

ABSTRACT

As major IP blocks such as GPUs increasingly dominate the area, power and performance of next generation SoCs, traditional “Soft IP” fully synthesisable, process-neutral solutions need to be re-evaluated to maintain the optimum balance between maximum portability and maximum performance. In this paper, we will discuss the techniques being used by Imagination and its partners to address some of the highest performance corners of this envelope, and how the characteristics of the latest processes such as 28HPM and beyond are being taken increasingly into account when designing future Soft IP high performance solutions.





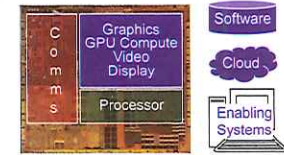
Imagination Technologies: Implementing and Optimising Graphics IP in SoCs

www.imgtec.com

Company overview



- **Leading silicon, software & cloud IP supplier**
 - Graphics, video, audio, communications, processor, cloud
 - Licensing and royalty business model
- **Licensed to many top 20 semis & OEMs**
 - Servicing high volume, high growth markets
- **Shipped by most major consumer brands**
 - Smartphones, tablets, TVs/STBs, games consoles
 - Radios, connected audio & video devices
 - Automotive dashboards, navigation, communication
- **Strategic product division: Pure**
 - Digital radio, internet connected audio (today)
 - IP business pathfinder, market maker
- **Established technology powerhouse**
 - Founded 1985; London FTSE250 (IMG.L)
 - Employees: 1,200+
 - UK HQ; operations world-wide
 - Global customer base



Technology Division:
Solution Centric IP

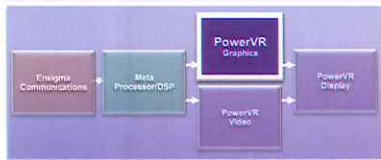


2

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PowerVR GPUs - graphics & compute

Leading the mobile and embedded graphics market



- **3D graphics: triangles to pixels**
 - User Interfaces; Games; Navigation
 - Accelerating Flash, HTML5
- **2D graphics: drawing windows**
 - UI windows; "composition"
- **GPU Compute**
 - Image processing; augmented reality; physics; face & gesture recognition
- **Industry Standard APIs**
 - 3D graphics: OpenGL ES; OpenGL; DirectX
 - GPU Compute: OpenCL
 - 2D: OpenVG; EGL
 - Ray Tracing: OpenRL™

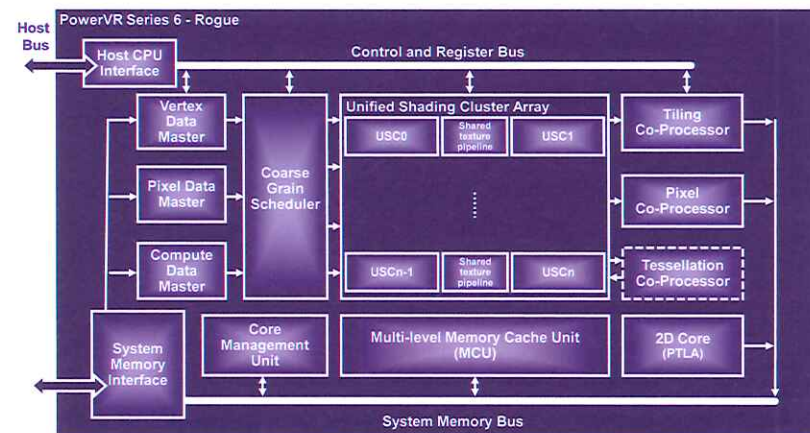


3

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Industry-leading embedded graphics

PowerVR Rogue Block Diagram



4

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GPU increasingly dominates SoC processing

GP-GPU

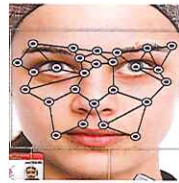


GPU compute

- Parallel compute on Graphics Processing Units (GPU)
- Efficient use of GPU compute arrays to handle complex calculations leaves CPU cycles for less specialised tasks

Use cases include:

- Image processing
- Video pre/post processing
- Augmented reality
- Physics
- Face & gesture recognition



Facial gesture detection



Augmented Reality (image courtesy String)



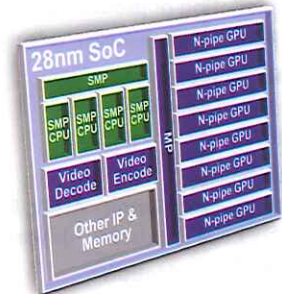
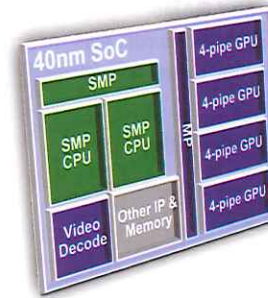
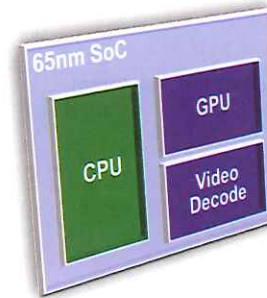
Advanced physics – fluid dynamics

5

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GPU increasingly dominates SoC processing

Data parallel architectures



- GPU multi-processor and multi-pipe configurability enables far more extensive processor scaling than CPUs
- SMPs unlikely to scale past 4 CPUs

OpenCL unlocks the enormous processing potential of GPU Compute

6

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A growing trend

Ray tracing



- Moves image quality to the next level
- Demands an even greater proportion of system capacity, e.g. bandwidth

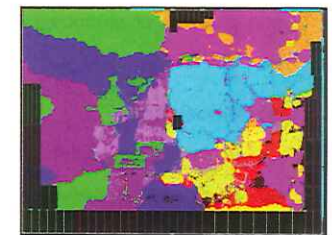
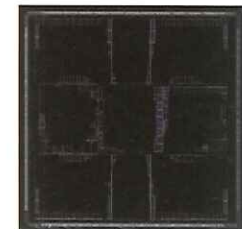
7

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Graphics IP - design for implementation



- Graphics IP is challenging for physical implementation teams
 - Many million instances in multi-block hierarchical layouts
 - Complex floor planning – multiple RAMs, arithmetic pipelines, interconnect
- IP has to be developed within a physically aware flow
 - Early prediction and avoidance of congestion
 - Careful handling of large mux and switch structures
 - Staging registers for block to block interconnect
 - Accurate prediction of Power/Performance/Area
- Reference methodologies are needed
 - Floor plan guidelines
 - Synthesis and layout scripts
 - Constraints



8

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Graphics IP - optimisation



- **Product differentiation is through better IP implementation**
 - Best power/performance/area will win
 - Trade-off between design effort/time and level of optimisation (e.g. hierarchical vs. flat design)
- **Optimised standard cell libraries and RAMs**
 - Tuned for critical paths such as cache RAMs and data path
 - Mega cells, fine grained cells, special cells, setup / hold trade-off
- **Exploitation of process capabilities**
 - Multi Vt, channel length, voltage scaling, overdrive
- **Data path optimisations**
 - Custom algorithms
 - Relative placement
- **Design flow**
 - Pessimism reduction – AOCV, library characterisation
 - Clock tree optimisation – power reduction, useful skew
- **Power optimisation**
 - Clock gating, voltage and frequency scaling, power islands, thermal monitoring

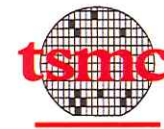
9

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Imagination / TSMC collaboration



- **Significant activities underway between Imagination and TSMC to fully optimise all of Imagination's IP cores on TSMC's 28nm and below processes**
- **Initial focus on PowerVR GPU PPA optimisation on 28HPM**
 - Gains of up to 15% being seen using optimised TSMC standard cell and memory libraries
 - Our thanks for great work by engineers from TSMC
- **Membership of Soft IP alliance now being expanded to all members of Imagination's IP portfolio**
 - PowerVR graphics GPUs
 - PowerVR video VPUs - multi-standard decode and encode
 - Meta CPUs - embedded processor/DSP
 - Enigma RPU - multi-standard TV/radio receiver & Wi-Fi communications



10

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Conclusions



- **The GPU is an increasingly dominant element in an SoC**
 - Provides a growing proportion of the total processing capability in the system
 - Modern graphics applications demand a large proportion of system resource
- **GPU design and implementation complexity increasing**
 - Growing challenge of maximizing IP portability while achieving best possible performance
- **Collaboration is key**
 - GPU IP providers must work closely with semiconductor companies and customers
 - A more holistic design approach is required

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NOTE

This image shows a single sheet of white paper with horizontal ruling lines. The lines are evenly spaced and run across the width of the page. There is no text or other markings on the paper.

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Advanced Silicon Design Methodology For Achieving 20nm Ready, Physical IP

Synopsys

ABSTRACT

The impact of the 20nm process on physical IP such as DDR4, PCI Express 3.0, USB 3.0 and data converters has its benefits and challenges to the design team. The benefits include higher transition frequency and more transconductance of the transistor that enable faster designs with more gain. Migrating to the 20nm process also gives designers the opportunity to re-design architectures to improve the power, performance and area. The challenges of migrating include adapting to new layout requirements that involve supporting double patterning technology (DPT), density requirements for metal and polysilicon as well as lower transistor output conductance .

Synopsys has developed an advanced silicon test-chip design methodology which solves two fundamental challenges of enabling 20nm ready physical IP. The first is related to the CAD flow: the verification decks for design rule checking, metal filling and restricted density design rules below metal one, require significant changes to the infrastructure and management of the design database compared to 28nm. The purpose of this methodology is to prepare a 20nm “pipe-cleaner”, enabling faster design of the complex physical IP. Due to aggressive time-to-market schedules, customers are expecting guarantees that the physical IP works on the first instantiation. The second and larger challenge, which is addressed in the test-chip, is the need to correlate between SPICE simulations and silicon characterization data of the fundamental IP blocks such as transistors, capacitors and resistors of various aspect ratios. This activity can only be achieved through extensive collaboration with TSMC, as a member of its OIP program.

A statistically meaningful number of devices must be chosen to ensure the simulation-to-silicon correlation, equating to 1500 devices with different layouts and density dependencies that provide data for resistor / transistor matching and metal mismatch due to DPT. Ring oscillators and operational amplifiers give early insight into the gate delay and analog performance of the 20nm process. Metal-in-Metal (MiM) capacitor structures are also used. The test-chip design methodology also includes overstressing devices to evaluate the impact on reliability due to NBTI, PBTI and HCI. Electro-static discharge (ESD) structures are a part of the physical IP and need to be designed for the human body model (HBM) and charged-device model (CDM) performance. For example, CDM must be tested across different voltage domains. In order to achieve USB 2.0 and HDMI compliance in the 20nm process, the I/O must support 5 V and implement the necessary ESD structures. DDR4's single-ended I/O running between 2400 Mb/s and 3200 Mb/s provides a unique design challenge and this is included in the test-chip.

A current-to-voltage voltage converter for measuring the devices with better than 0.5% accuracy acts as the on-chip instrumentation, which is more than adequate for devices that typically have greater than 20% mis-match. A 4-pin JTAG interface allows full visibility and enables 1500 devices to be tested in under two minutes.

Using design and simulation examples with silicon correlation, this presentation will describe the challenges and solutions of creating high performance physical IP using this advanced silicon design methodology.

Advanced Silicon Design Methodology For Achieving 20-nm Ready, Physical IP

Navraj Nandra

Senior Director, Analog/Mixed-Signal IP

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Presentation Objective

New silicon design methodology for 20nm physical IP

1. New physical IP architectures

Designed to meet power, performance, area (PPA) targets with aggressive time to market, developed on an early PDK, no re-use of previous designs

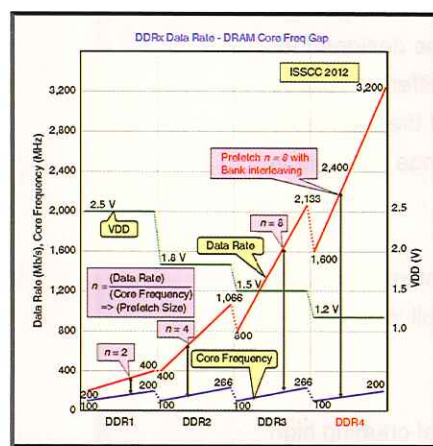
2. Advanced silicon design methodology

- Executed on Technology Assessment Chip
- Develop and pipe-clean new CAD infrastructure
- Correlate the simulation of the fundamental devices to silicon data, that make up the new physical IP

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LPDDR3 – Drives Foundry I/O Strategy DDR4 – Drives Speed



PPA target: DDR4 speed; LPDDR3e speed/low power

Specifications

- Evolving serial/parallel termination schemes
 - DDR4 is series + parallel to VDDQ
 - LPDDR3 tries to avoid termination all together
- Single ended interface
- DDR4: 1.2V 3.2 Gb/s
- LPDDR3e: 1.2V 2133 Mb/s
- Need larger pre-fetch size, bank interleaving

20-nm design challenges

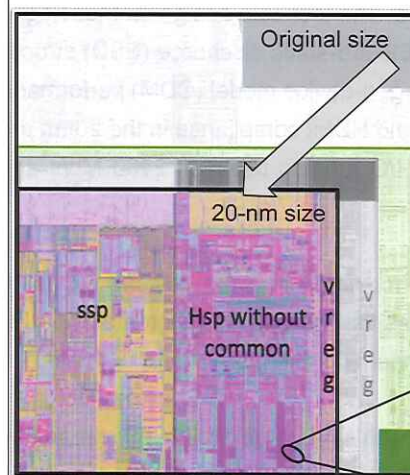
- Better density, but V_t not scaling
 - Hard to support 1.2V with thick-ox I/O
 - Issue compounded by variable V_{ref} (LPDDR3)

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USB 3.0, 20nm 1.8V I/O

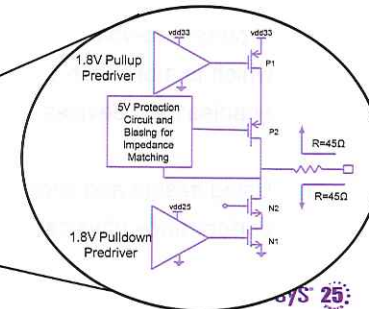
Smaller area and electrical compliance must be met



PPA target
Area reduction; 5V battery charging; all 4 USB speeds

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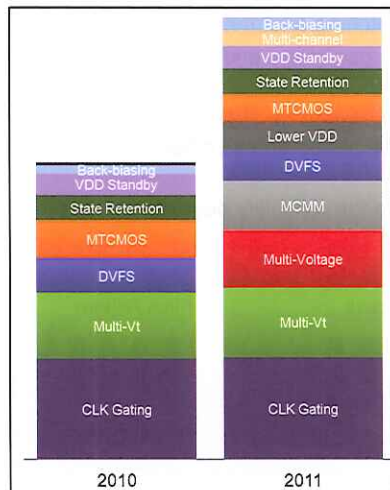
- Must support all four USB speeds:
5 Gb/s, 480 Mb/s, 12 Mb/s, 1.5 Mb/s
- 5 V USB electrical compliance requirement
 - Must be met using devices 1.8 V devices
 - Guaranteed device reliability meeting 3.3 V signal swings during Full Speed & Low Speed USB operation
 - Successfully operates after shorting the differential signal pair to 5 V for 24 hours
- NBTI (high voltage overstress) will impact receiver squelch threshold → causing electrical compliance failure



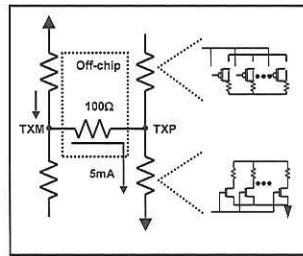
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PCI Express: Lowering Power

Design techniques plus new specs



PPA target: speed, new low power modes



Low-power design techniques

Multi-voltage, multi-channel, SVS, retention

Low-power architectures

Voltage mode for PCIe 2.0

Hybrid mode for PCIe 2.0, PCI 3.0

New PCI Express specifications

System, sleeping states (S0 – S5)

Device power states (D0 – D3)

Link power states (L0 – L3)

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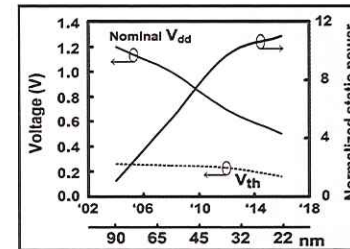
Source: 2011 Synopsys Global User Survey. May only be used with authorization from Synopsys.

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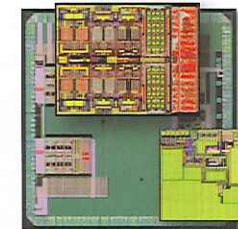
Data Converters

Meeting dynamic range

- Supply voltage almost halved from 65nm to 20nm
- Analog video / audio dynamic range > 1.3V means no voltage headroom for high linearity @ 1.8V supply
- Flicker (1/f) noise inversely proportional to transistor length (L)
→ if L reduced 5X, to reserve the same SNR, area needs to increase 25X
- New analog techniques: clock boosting circumvents low supply voltage, internally processing signals with large voltage swings



Source: ITRS roadmap, supply voltage and threshold voltage



Synopsys : LTE analog front-end using 1.8 V

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20nm PPA Requirements

IP Specifications:

- DDR4, LPDDR4 → higher I/O speeds using single-ended interface
- USB 3.0 → must support all 4 speeds, meet electrical compliance
- PCI Express → 5 Gb/s, 8 Gb/s but support new low power modes
- Data converters → dynamic range versus lower voltage headroom

Market requirement:

- Physical IP scales (area, power) without performance degradation
- Supports aggressive schedules → designed on an early PDK
- Works on first instantiation in SoC



Requirements: advanced silicon design methodology and close co-operation with foundry

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20nm Layout Dependent Effects

Semiconductor processing requirements

- WPE
- LOD
- OSE
- PSE
- PO.DN.15
- Pattern Density Effect
- OPC (Optical Proximity Check)
- GDA (Gross Die Advisor) Criteria
- MFU (Mask Field Utilization) > 80%
- DFM LPC (Layout Patterning Check)
- HCI (Hot Carrier effect Injection)
- Dummy OD (DOD) rules
- Dummy Poly (DPO) rules
- SM (Stress Migration)
- NBTI
- PBTI
- PSM
- RTO

PPA requirements for Physical IP

Technology assessment chip

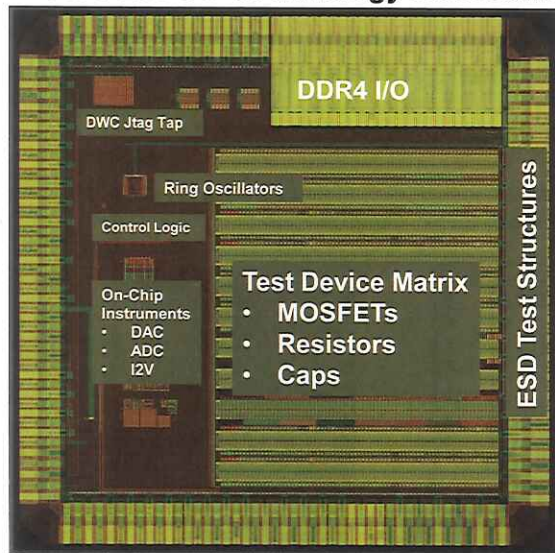


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Enabling Robust 20nm IP Development

TSMC 20SOC Technology Assessment Chip



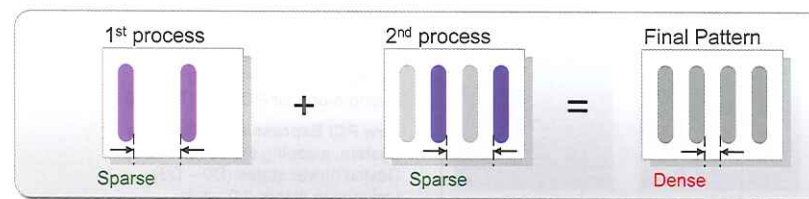
- 20nm CAD flow pipe cleaner
- Correlate to simulation
- Fundamental IP structures:
 - Ring oscillators
 - DDR4 I/O
 - Analog IP
 - Test devices

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Technology Assessment Chip

- **DPT:** 1500 devices with different layouts and density dependencies providing data for resistor / transistor matching and metal mismatch
- **Analog performance, gate delay:** Ring oscillators and operational amplifiers give early insight
- **Electro-static discharge:** Need to be designed for HBM and CDM performance – for example CDM must be tested across different voltage domains
- **Ability to overstress devices:** Evaluate the reliability degradation due to NBTI, PBTI and HCI

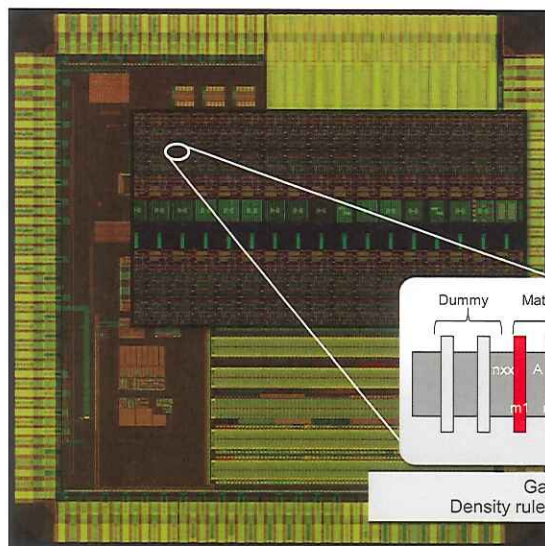


Dense pattern can be split into two sparse patterns

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Test Matrix



- On-Chip
- Device-Under-Test matrix
 - I-to-V conversion
 - DAC
 - Current compare
 - Fast BIST testing
 - 1,500 test devices
 - Matching & density aware

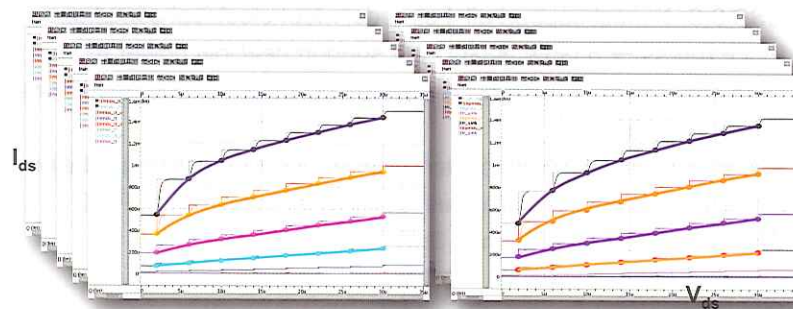
Gate Matching guidelines
Density rules optimized for analog matching

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20nm MOS characteristic: Classic IV Sweep

- Test device: NMOS/PMOS: 2.7 μ m/0.018 μ m
- TR simulation: V_{gs} (0.3V \rightarrow 0.9V) & V_{ds} (0.1V \rightarrow 0.9V) sweeping
- I_d range: 180 nA \rightarrow 1.50 mA



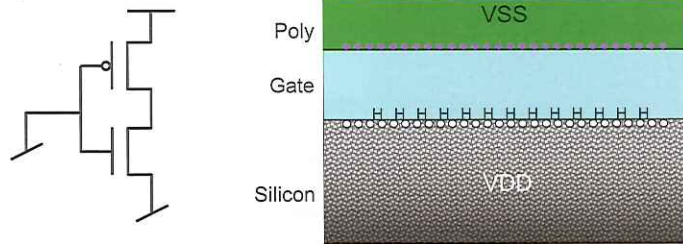
Walk sequentially through all 1,000 devices

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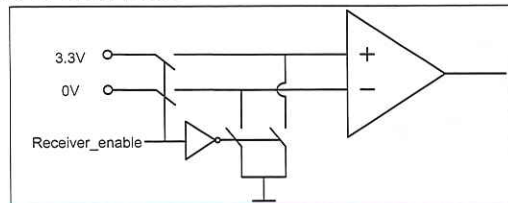
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Example of a Simple Circuit Issue

Simple circuit



USB Example of NBTI Issue

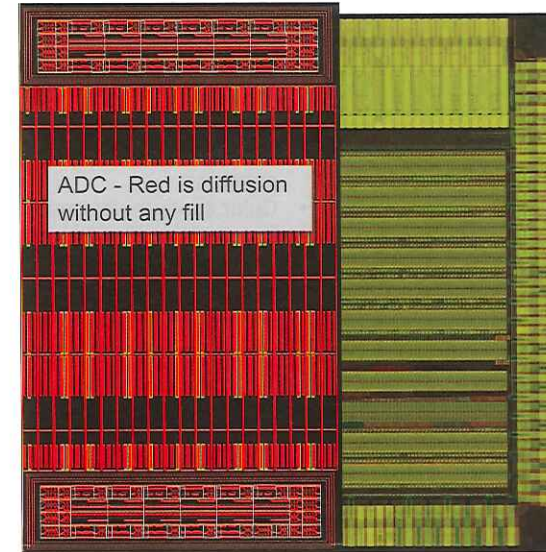


Mitigation of the NBTI problem:
Introduction of symmetric stress on both inputs to the differential pair by pulling input to the same voltage during suspend mode.

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Layer Densities on 20nm (Pre-fill)



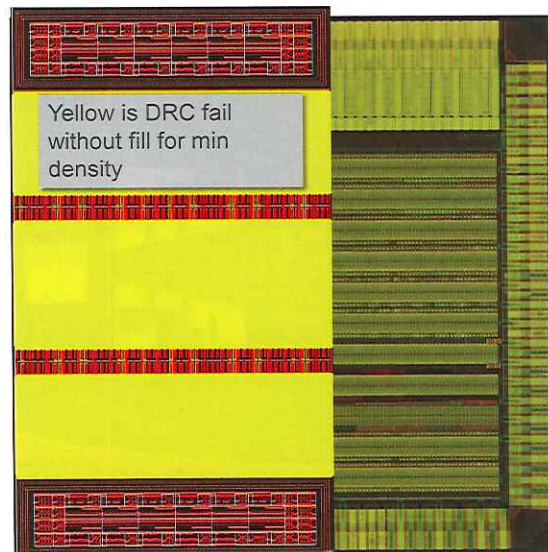
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On-Chip ADC example

- Requires good matching for both MOSFET's and resistors
- Strict density requirements per layer in "walking window"
- For example, DIFFUSION density must be >20% in 18μm window & < 80% in 100μm window
- BUT, critical matching depends on actual density variations b/w 20% & 80%
2 devices are not identical unless they are in areas of identical density on >1 layer

SYNOPSYS 25

Layer Densities on 20nm (Pre-fill)



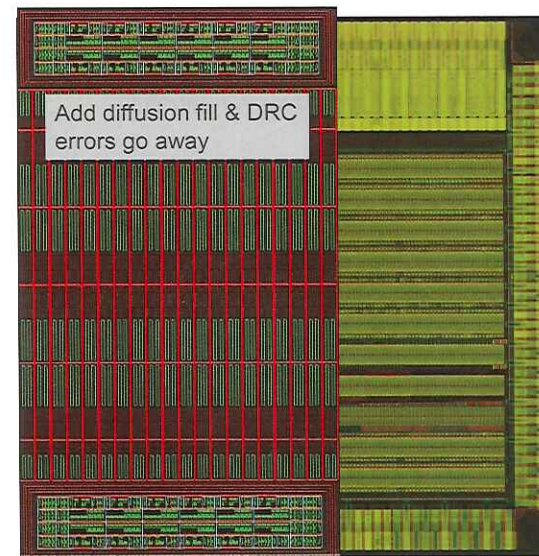
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On-Chip ADC example

- Requires good matching for both MOSFET's and resistors
- Strict density requirements per layer in "walking window"
- For example, DIFFUSION density must be >20% in 18μm window & < 80% in 100μm window
- BUT, critical matching depends on actual density variations b/w 20% & 80%
2 devices are not identical unless they are in areas of identical density on >1 layer

SYNOPSYS 25

Layer Densities on 20nm (Filled)



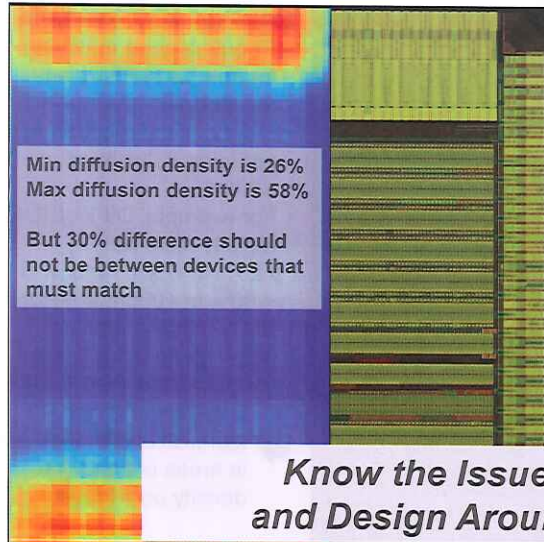
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On-Chip ADC example

- Fill will increase density in areas where it is too low
- But you need to "see" the actual density for matching

SYNOPSYS 25

Layer Densities on 20nm (Filled)



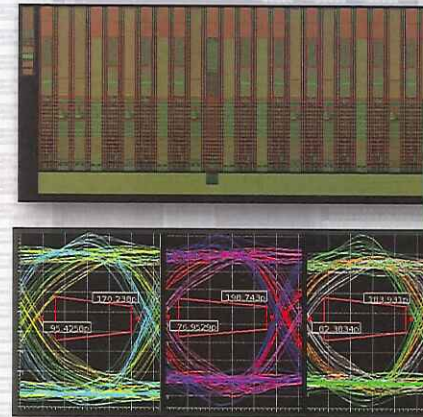
On-Chip ADC example

- Fill will increase density in areas where it is too low
- But you need to “see” the actual density for matching
- Color contour plot on the layout shows the actual window densities
- The MOSFETs in the bottom of the DAC should all be in a uniform density to get good silicon performance

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SYNOPSYS 25

DDR4 I/O – Overcoming 20-nm Design Challenges



Implement:

- Novel circuits designed to meet DDR4 as well as legacy DDR3 (wide IO range)
- Pre-emphasis – to help with SI-based losses
- Improved Rx to deal with closed eyes

Feasibility Results
Showing pre-emphasis performance for
DDR4 needs above 3.2 Gbps rates

Technology Assessment Chip

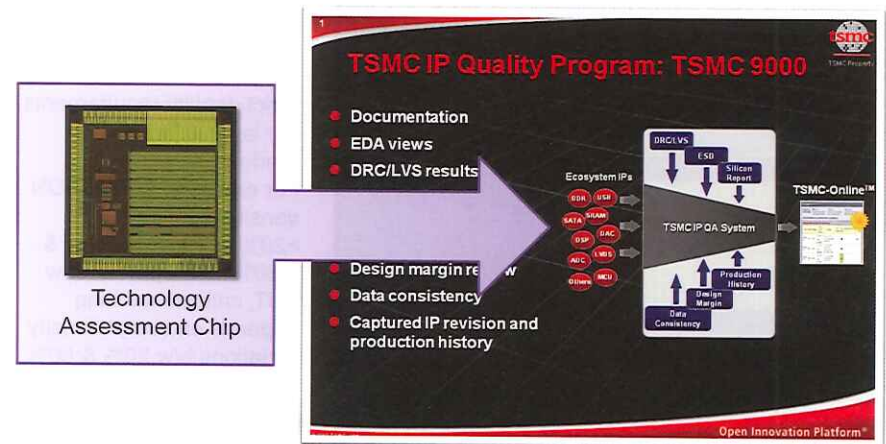
Key Points

- Technology assessment chip was designed on a very early PDK
 - Methodology had to adapt to known / unknown variations in PDK
 - Highly experienced engineers (analog, mixed-signal, layout, process, CAD) that could handle the uncertainty did the development
- 1,500 devices – impossible to layout manually and be able to absorb the PDK changes → automation was key
- CAD flow pipe cleaning (fill, DRC) significantly helped in meeting the next set of 20nm physical IP tape-outs
- Underestimated post-fill DRC run-times
(there are a lot of fill rectangles on a 20nm, 2mm x 2mm die one billion rectangles...)

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Synopsys and TSMC OIP Collaborating for 20nm Physical IP Success



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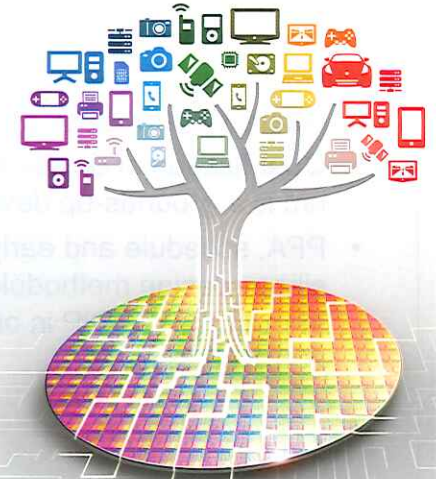
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Summary

- 20nm requires a much deeper link between layout and performance than in previous nodes
- Double patterning and its effect on circuit density under different metal stack conditions must be considered
- Quantization of device sizes means no 28nm re-use, 20nm is a grounds-up development
- PPA, schedule and early PDK necessitates an advanced silicon design methodology with close co-operation through TSMC OIP in order to build successful 20nm physical IP

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The Trusted Technology and Capacity Provider



Comprehensive Embedded NVM Solution in Trusted Technology and Capacity Platform eMemory

ABSTRACT

eMemory, as a pioneer in the eNVM IP segment with 170+ patents granted and more than 2,000,000 wafers shipped in TSMC, has built a sterling reputation by offering total solutions with its proprietary OTP, Pseudo-MTP(PMTP), MTP, EEPROM and emb-Flash technologies. With the support of TSMC's "More-than-Moore" technologies, eMemory can offer customers maximal design flexibility and the greatest range of choices in process platforms, enabling product differentiation and giving customers a competitive advantage in the rapidly changing industry. Drawing on eMemory's extensive experience and robust design capabilities in technology and IPs, TSMC 9000-warranted IP deliverables can be deployed for commercial, industrial, and automotive applications. With its supreme quality and excellent customer services, eMemory received 2011 TSMC Best IP Partner Award which is for the second year in a row. It acknowledges eMemory's technical ability, long-term involvement in customer projects and commitment to quality.

eMemory's proprietary OTP (NeoBit) macros, besides wide availability in mature process nodes, have been released successfully on TSMC's 80nm HV process for production. In the mean time, NeoBit is being developed on 130nm BCD process for the purpose to meet the requirement of next-generation mobile devices for better power management. In addition to NeoBit IP availability, eMemory's proprietary single-poly MTP (NeoMTP), single-poly EEPROM (NeoEE) and single-poly SONOS Flash (NeoFlash) are also being developed in different TSMC process nodes.

NeoBit is a programmable logic device offering the industry's most proven path to embedded OTP and PMTP functionality. The usages of NeoBit IPs can be found in power management ICs, HD720 LCD driver ICs, audio CODE ICs, and MEMS in smart phones. Based on the wide process availability and maturity in NeoBit, NeoMTP, a derivative structure of NeoBit cell for operations of electrical programming and erase, can be soon ready in all NeoBit process nodes. The key feature of NeoMTP is suitable for Touch-panel controller (TPC), NB CAM controller, ASSP MCU, and fuel-gauge IC.

NeoEE serves as a well rewritable memory technology with simple but robust architecture, supporting up to 100K P/E cycles without additional mask layers. The core functionality of NeoEE is promising for IC cards with user preference settings, ID storage in RFICs, and NFC-based electronic wallets. Highly reliable quality, endurance, and data retention make NeoEE a superior alternative to traditional external SPI flash or I2C EEPROM.

This presentation is organized into several sections. In the 1st section, it describes eMemory's eNVM capability and availability in a broad range of TSMC process nodes to fulfill customer requirements for blooming product applications. The 2nd section introduces eMemory's core technologies, target markets and key features. eMemory's infrastructure of technical support to TSMC and its customers, technology porting to a variety of processes, and customized design capabilities are outlined in the last section.





Comprehensive Embedded NVM Solution in Trusted Technology and Capacity Platform

Michael Ho

Sr. Director of Sales and Marketing Division

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eMemory

Outlines

- **About eMemory**
- **Comprehensive eNVM Solutions in TSMC OIP**
- **Core Technology and Target Markets**
- **Customer Benefits, Technical Support and Service**
- **Summary**

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eMemory

Corporate Overview

- eMemory is a logic NVM IP provider with complete OTP, PMTP, EEPROM, MTP and Flash solutions
- **150+** NVM IP developers out of 190 employees*.
- Completed patent portfolio: **170+** patents issued, **120+** pending
- Number of IP verified: **550+**
- Number of New Tape Outs: **1750+**
- Productions: **4,400,000+** wafers shipped thru Q2'12
- Foundry coverage: **TSMC** and other 15 foundries worldwide
- IDM coverage: **10** IDMs worldwide

* Source by July., 2012

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IP Partner Award Winner



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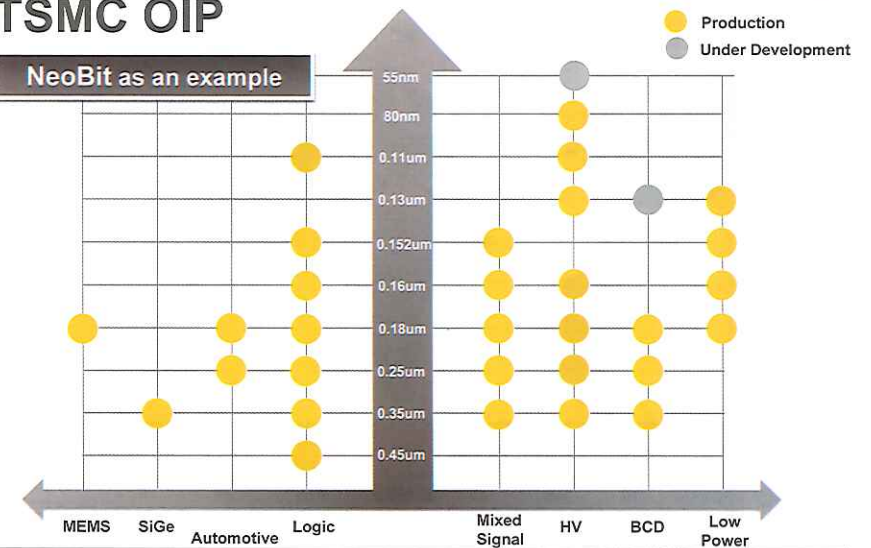
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Comprehensive NVM Solutions in TSMC OIP

NeoBit as an example



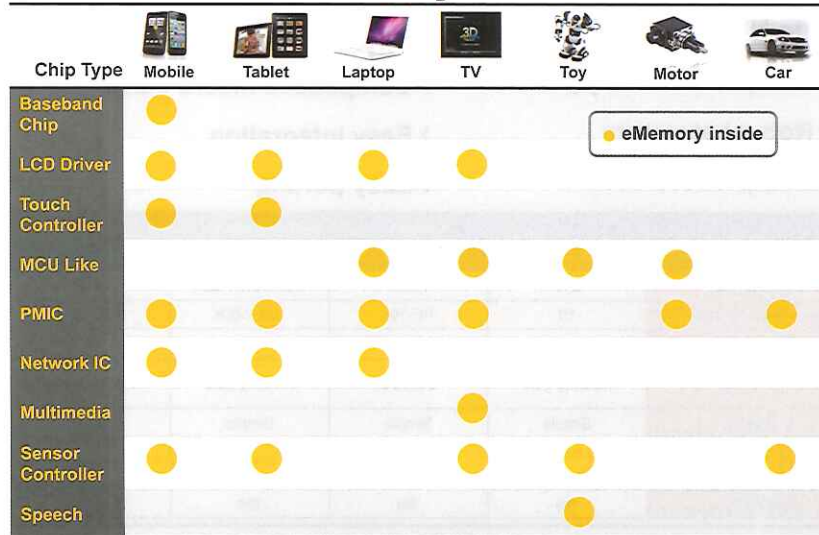
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Embedded Everywhere



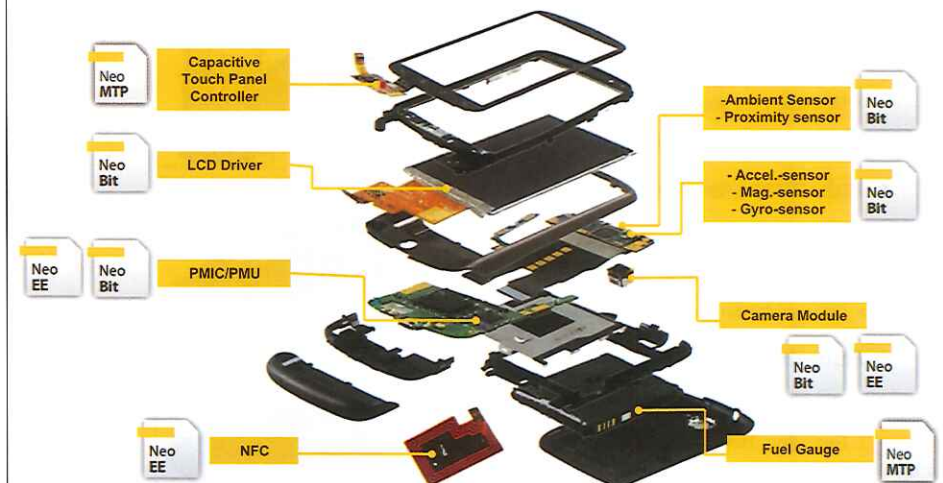
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Smart Phone ICs with Our NVM IP



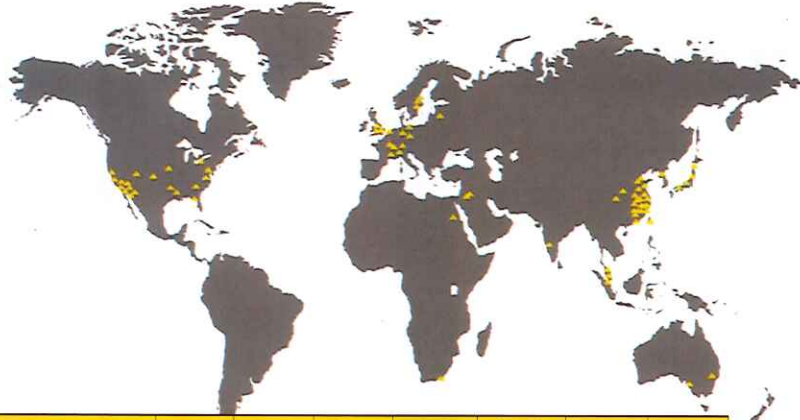
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Worldwide Tape Outs



New Tapeout Counts (2010Q1~2012Q2)	Taiwan	China	Korea	Japan	North America	Europe	Others
Fabless NTO by Region	330	120	35	23	109	84	5

Source as of July, 2012

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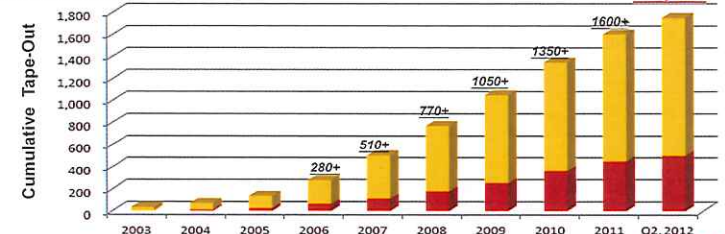
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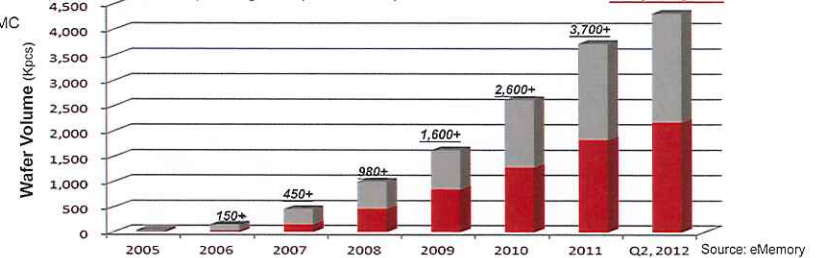
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Innovation for Wide Utilization

■ NTO in the corresponding Year (as of Q2'12)



■ Wafer Shipment in the corresponding Year (as of Q2'12)



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Full Quality Coverage

• Commercial grade NeoBit

- › Operation range: -40°C ~ 125°C
- › Retention: 10 years @ 85°C
- › Standard offering for NeoBit IPs



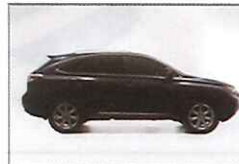
• Industrial grade NeoBit

- › Operation range: -40°C ~ 125°C
- › Retention: 10 years @ 125°C
- › Only available on specific processes



• Automotive grade NeoBit

- › Operation range: -40°C ~ 150°C
- › Retention: 10 years @ 125°C
- › Zero failure
- › TSMC only



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eMemory's NVM Technologies

Logic NVM solutions constitute a complete platform

- › Compatible to any process
- › Competitive macro sizes
- › Robust structure
- › Easy integration
- › Low process cost
- › Easy porting

eMemory's NVM Technology	Comprehensive NVM Solutions			
	NeoBit	NeoFlash	NeoEE	NeoMTP
Product Type	OTP	Flash	EEPROM/Flash	MTP
Endurance (Cycles)	10	1K~10K	10K~100K	1K~10K
Additional Mask Steps	0	2-3	0	0
Technology	Floating gate	SONOS	Floating gate	Floating gate
Scalability	Simple	Simple	Simple	Simple
Memory Density	HD < 512Kb GHD < 16Mb	< 2Mb	< 16Kb	< 512Kb
Testability	Yes	Yes	Yes	Yes

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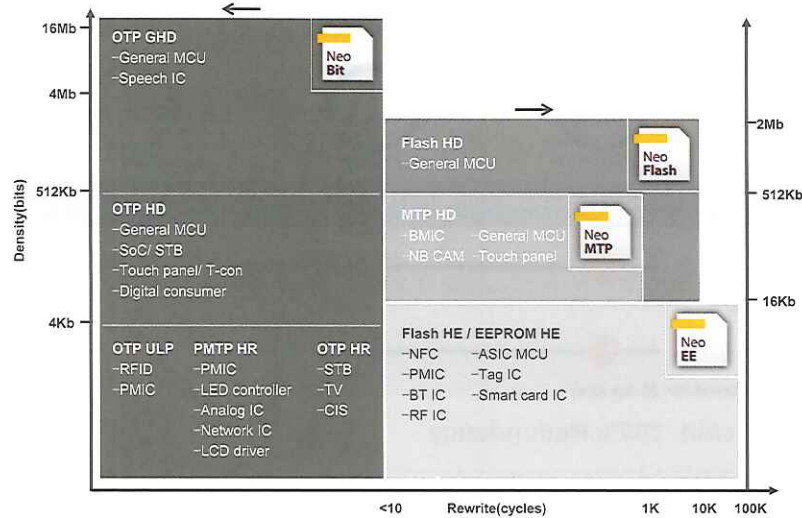
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Innovation Technologies

Wide selection of embedded NVM cover many application



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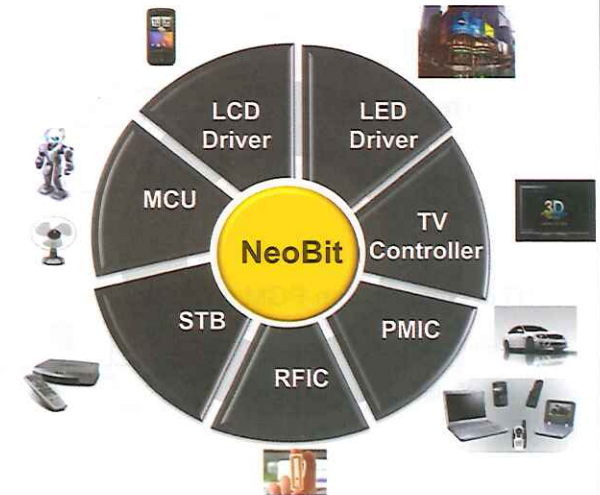
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NeoBit Market Applications

NeoBit Key Highlights

- > 55nm HV for Full HD DDI
- > 80nm HV for HD720 DDI
- > 130/180nm BCD for mobile PMIC
- > 180nm MEMS for Smart sensors



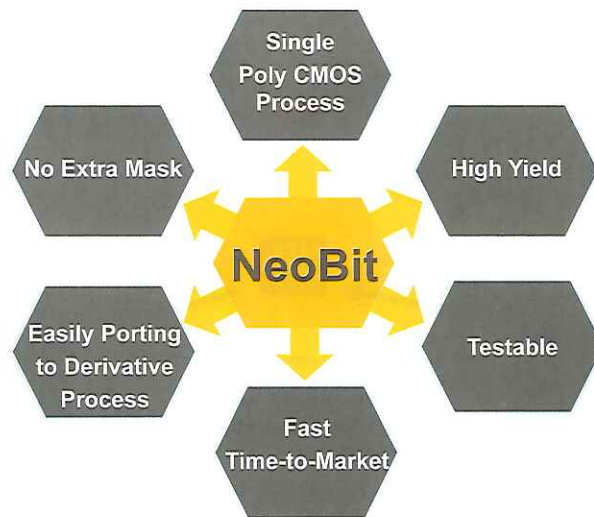
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NeoBit Advantages



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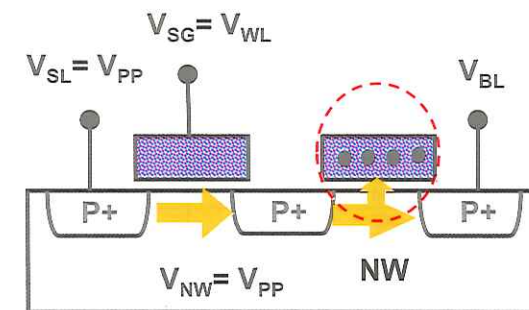
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Programming Operation

- Programming by channel hot electron injection
- Floating gate potential is induced by charges within and coupled by the voltages at BL, SL, and NW



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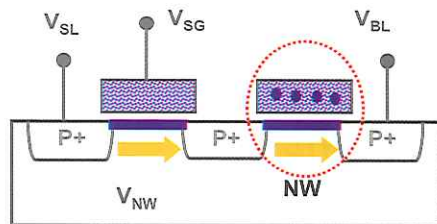
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Read Operation

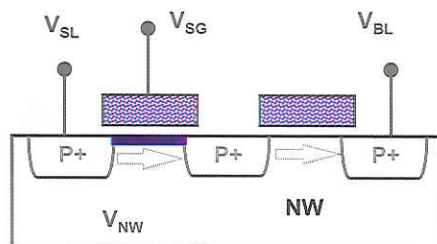
- FG is charged after PGM

- › Cell is on
- › High read current



- FG is empty in non-PGM cell

- › Cell keeps off
- › Negligible leakage current



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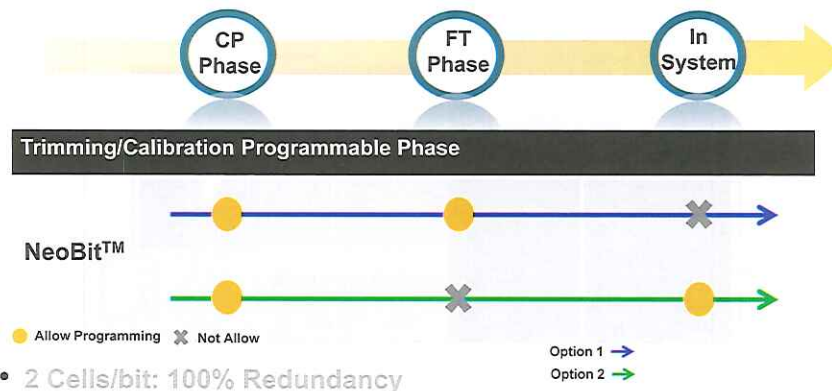
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NeoBit - the High Yield Solution

- Testable:

- › Lowest cost risk at CP and keep product flexibility at FT or System



- 2 Cells/bit: 100% Redundancy

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The 1st Automotive Grade

- Qualification Plan Follows AEC-Q100
- Zero Failure

Test Item	Sample Size per lot	# of lots	FT condition	Criteria Acc/SS	Result
Pre conditioning	77 for THB,AC,TC	3	RT	0/715	Pass
	22 for PTC	1			
Temperature Humidity Bias	77	3	RT+HT	0/231	Pass
Auto Clave	77	3	RT	0/231	Pass
Temperature Cycle	77	3	HT	0/231	Pass
Power Temperature Cycle	45	1	RT+HT	0/45	Pass
HTOL	100	3	RT+CT+HT	0/300	Pass
ELFR	800	3	RT+HT	0/2400	Pass
HTS	77	3	RT+HT	0/231	Pass
ESD(HBM)	96	3	RT+HT	0/288	Pass
ESD(MM)	96	3	RT+HT	0/288	Pass
LU	6	3	RT+HT	0/18	Pass



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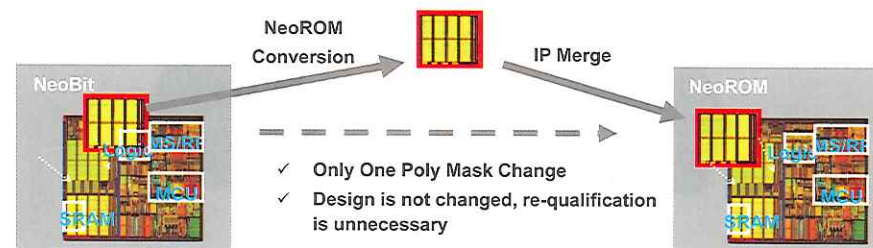
NeoROM Service

- OTP for Prototyping

- › Fast Time-to-Market
- › Flexible Program Code

- ROM for MP

- › Reduce Test Cost
- › Self-Certificated



- ✓ Only One Poly Mask Change
- ✓ Design is not changed, re-qualification is unnecessary

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Product Family and Application

Neo Bit

			0.13um			
		0.18um	55nm 0.18um	0.18um	0.13um	
Technology	65nm 0.25um	65nm 0.25um	0.25um	0.18um	0.18um	
	80nm 0.35um	80nm 0.35um		0.25um		
	0.13um 0.5um	0.11um 0.5um	0.35um	0.25um		
Product	OTP-HD	OTP-HR	OTP-ULP	PMTP-HR	OTP-GHD	
Density	4K ~ 512K bits	8 ~ 4K bits	256 ~ 4K bits	32 ~ 4K bits	4K ~ 16M bits	
Applications	✓ MCU ✓ Consumer ✓ Touch Panel	✓ Analog IC ✓ LCD Driver ✓ PMIC	✓ RFID	✓ Analog IC ✓ LCD Driver ✓ Consumer	✓ Speech IC ✓ General MCU	
Function	✓ Code Storage ✓ ROM ✓ Replacement	✓ Encryption ✓ Code Storage ✓ Trimming ✓ Parameter ✓ Setting	✓ RFID Code ✓ Storage ✓ ID Setting	✓ Trimming ✓ Parameter ✓ Setting	✓ Data or Code Storage ✓ ROM Replacement	

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TSMC Production Processes

Neo Bit

NeoBit Technology						
0.45um	5V					
0.35um	3.3/5V	3.3/5V	3.3/12V	3.3/+9V	3.3V	
	3.3V	3.3V	3.3/15V	3.3/12/15V	3.3/5/12/15/20/40V	
0.25um	2.5/3.3V	2.5/3.3V	2.5/5/20V	2.5/5/40V	2.5/5/60V	
	2.5/5V	2.5/5V	2.5/3.3/20V	2.5/5/40V	2.5/5/40V Enhanced	
0.18um	1.8/3.3V	1.8/3.3V	1.8/6/16V	1.8/5/40V	1.8/5/40V	
	1.8/5V	1.8/5V	1.8/5/32V	1.8/3.3V	1.8/3.3V MEMS	
0.16um	1.8/3.3V	1.8/3.3V	1.8/5/32V	1.8/3.3V		
0.152um	1.8/3.3V	1.8/3.3V		1.8/3.3V		
0.13um				1.5/5/6/32V	1.5/3.3V	
0.11um	1.2/3.3V Al+Cu			1.5/5/6/32V		
80nm				1.5/5/6/32V		

Logic Mixed-Signal High Voltage BCD SiGe Automotive Low Power MEMS

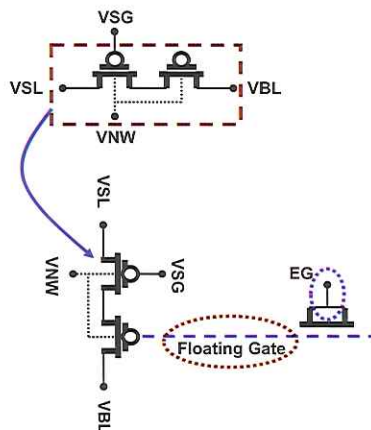
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eMemory MTP – NeoEE/NeoMTP

Neo EE



- NeoEE/NeoMTP is derivative from NeoBit
 - › CHI or FN – Program
 - › 1 Capacitive coupled GOX – Erase
- MTP Operation
 - › Program :
 - Channel Hot Carrier (NeoMTP)
 - Fowler-Nordheim (NeoEE)
 - › Erase:
 - Fowler-Nordheim Tunneling

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eMemory MTP Solutions

Neo MTP

- Simple and Reliable MTP Capability
 - › NeoEE/NeoMTP is a derivative of NeoBit technology and easily available on every NeoBit process
 - › Apply to process with 2.5V, 3.3V or 5V IO devices
 - › NeoBit cell with one coupling capacitor for erase operation
 - › 100% CMOS compatible process
 - › Memory density ranging from 1Kbits to 512Kbits
 - › Endurance from 100 to 10K cycles, depends on oxide integrity
 - › Compact and High reliable MTP Memory block

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MTP Development Schedule



* Right edge of each bar represents qual complete schedule



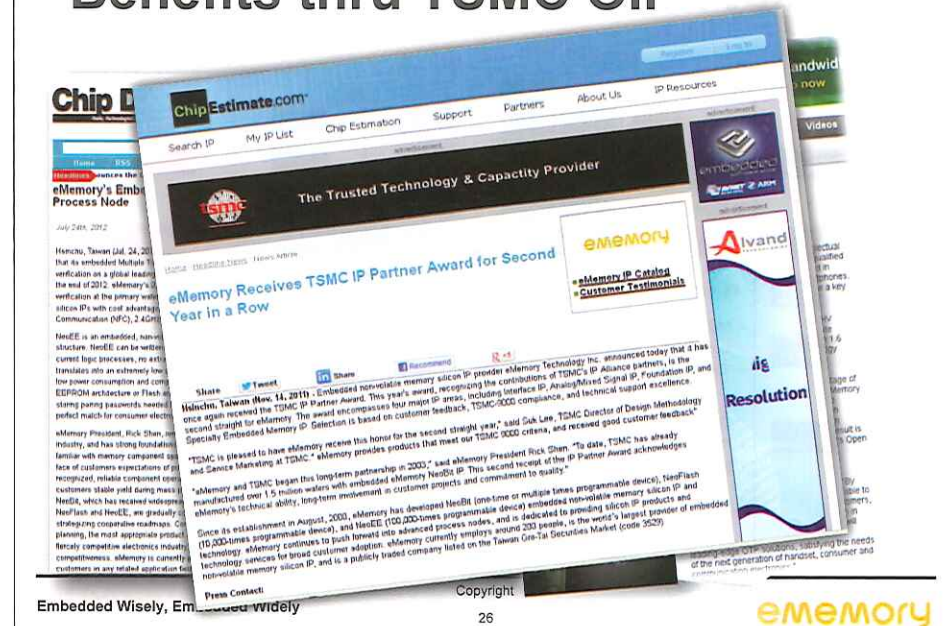
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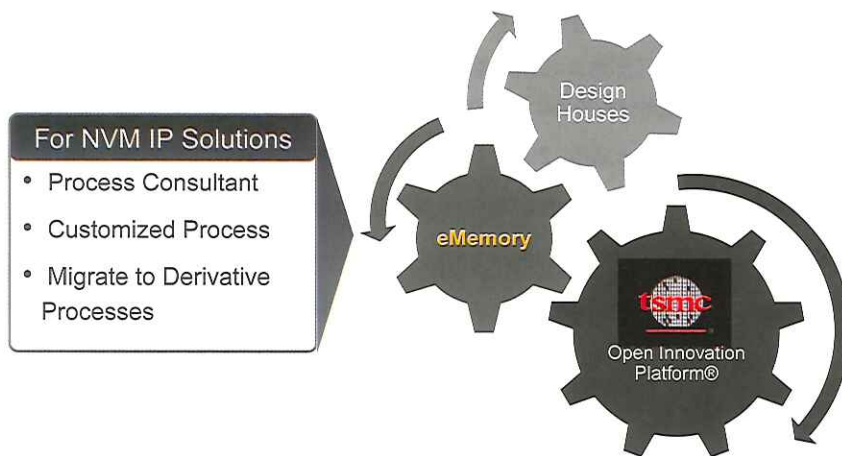
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Benefits thru TSMC OIP



Minimize Adoption Barrier



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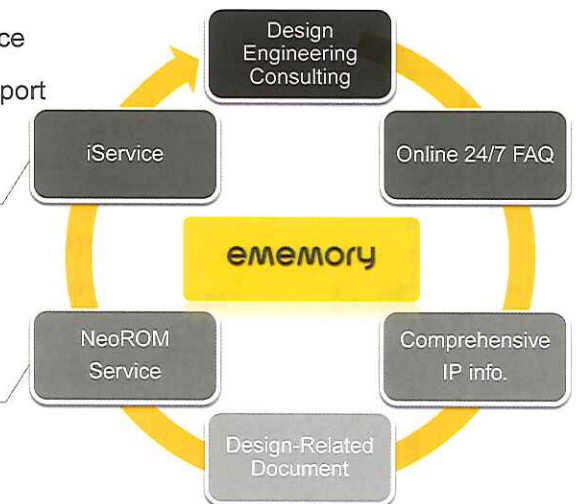
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Fulfills All You Need

- Flexible Design Service
- Strong Technical Support

- Downloadable Data sheets
- Complete Design Kit
- OTP (Design) → ROM (MP)
- Reduce Testing Cost
- Self-Certificated



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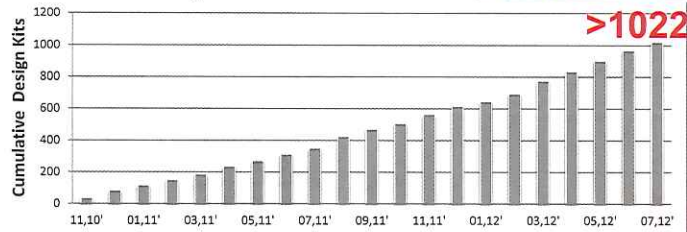
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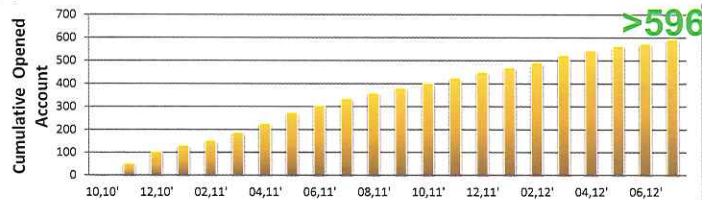
iService Performance

• Downloaded Design Kit

<http://iservice.ememory.com.tw>



• Applied Account



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NVM Expertise

Easily

Industry's easiest to implement embedded memory IP

Comprehensive

Comprehensive IP portfolio providing unmatched process portability

Extensive

Extensive fabless customer base ... over 400 active customers

Consult

Consult on process improvement

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Summary

- **One-Stop Shop Service for Comprehensive NVM Solutions on TSMC Trusted Technology Platform**
- **Logic NVM Solutions for Wide Utilization**
 - > NeoBit is well proven OTP/PMTP technology with full quality coverage
 - > NeoEE offers Flash/EEPROM capability in CMOS compatible process without extra mask
 - > NeoMTP is MTP solution with compact size and reliable performance in general CMOS process
- **Hybrid NVM Solution**
 - > Flexible design and cost effective according to development and production stages
 - > NeoBit + NeoMTP, NeoBit + NeoEE, and NeoROM + NeoEE

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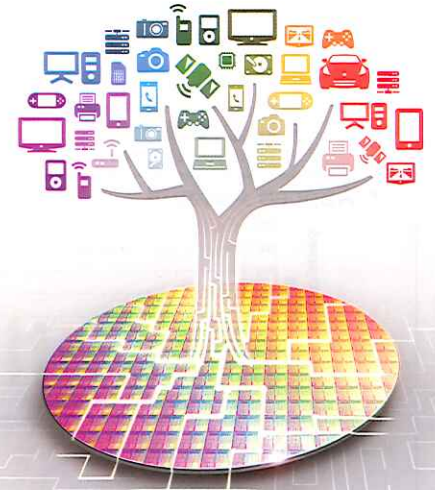
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Novel Low-Power Audio CODEC from 180nm to 28nm with Moore and More!

Dolphin Integration

ABSTRACT

Mature nodes, especially 180nm processes, are still widely used. The interest in these processes is reinforced by new flavors provided by manufacturers as BCD or eLL variants; which increases the spread of possible applications. One main concern with such processes is product cost, making the area more and more a critical parameter.

The choice of offering higher density audio codec, with a codec close to 1 mm², is driven by this trend. While the spread of process flavors is large, the design has to target all of them for the IP to be integrated in either pure logic, embedded flash or mixed-signal/RF variant. It also has to remain as independent from process options as possible, for neighboring either a small amount of logic functions or an RF emitter/receiver. The layout also must match different possible Top metal wire thicknesses.

As audio codecs are mainly used in portable applications, the reduction of power consumption is the next optimization criterion. The DAC achieves a 5 mW power consumption in playback configuration!

As higher audio performance is required, the DAC SNR has been increased to 95 dB. This overall trade-off between area, power consumption and performance is deemed best for portable applications.

The design has taken benefit of core transistors which have a better intrinsic noise than I/O transistors. They also enable denser analog designs with low power consumption, facilitating the reach of the 3 objectives.

To cover the wide range of configurations required by each specific customer's needs and to avoid penalizing the area, the FlexAudio method is applied. It is based on a pre-determined set of mixed-signal core and peripheral functions – for instance: ADC, DAC, input preamplifier and output amplifier -, which are then assembled to address the exact application needs, without unwanted and area penalizing functions. Thanks to this flexibility, a configuration can be extended easily with new peripherals.

One topic had to be faced regarding the logic design to deal with the trade-off between flexibility, scalability, complexity and form factor. As either the same analog front-end can be used with different logic options, or the same logic filtering can be used with different analog front-ends, the IP has been split in two parts through a dedicated interface, code-named “Bow”, enabling to significantly reduce the number of connections between the two parts. Splitting has additional advantages:

- It enables to independently place the analog front-end close to I/O ring and the logic part at the convenience of the integrator.
- As the number of connections required by the Bow interface is small, the logic part can be placed in another die enabling different evolutions of either the analog front-end or the logic part of the application without changing the other.
- The logic part can be processed with different process widths (from 180nm to 28nm...) in order to integrate the logic part with an application processor supporting high complexity applications.

Novel Low-Power Audio CODEC from 180 nm to 28 nm with Moore and more!

Frederic Renoux
Sales Director, Dolphin Integration

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Novel Low-Power Audio CODEC from 180 nm to 28 nm with Moore and more!

Agenda

- 1. Corporate Profile**
- 2. Market Trend and "More than Moore (MtM)"**
 - Evolution of Market Trend and Current Challenge
 - TSMC Process Technology in 180 nm
 - A Joint Force of TSMC & Dolphin
- 3. Engagement by Dolphin in the Market Challenge**
 - FlexAudio: Flexible Architecture
 - Bow & Chord Interface
 - EMBLEM-CTP: Transfer of Know-How
- 4. Best RoI Enabled by Dolphin and TSMC**
 - Helium3: Novel Audio 95 dB CODEC

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Novel Low-Power Audio CODEC from 180 nm to 28 nm with Moore and more!

Enabler of low power Mixed-Signal SoCs

2007 Power Management Network Solutions

1997 Model Libraries

2012 Transfer of SoC Integration Know-How

1985 Subsystem for Audio, Measurement, Storage & Microcontrol Logic and Cell Libraries

2009 Register Memories

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Market Trend and Current Challenge

Die Area

Process Node

Analog + Digital

Analog

PMIC

ROI

Design Time

Design Cost

Design Risk

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Market Trend and Current Challenge

Chipset Opportunity

- Best trade-off for integration safety & production cost
- Enabling more functionalities without scaling in advanced process

Die Area

Digital Part

Analog Part

180 nm 150 nm 130 nm 90 nm 65 nm 40 nm 28 nm

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A Joint Force of TSMC and Dolphin

Optimized Configuration

Low Power Consumption

Reduction of Integration and Application Risks

High Performance

Optimized Area

Shorter TTM

Low-Noise & High-Density Transistor

High Voltage Process

High Yield & Stability

p.6

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Unique Interfaces in Dolphin's Architecture of Audio CODECs

Chord: the interface between the ADC core and the DAC core, enabling an easy modulation

Bow: the interface enabling the split of the CODEC with a minimized number of pins:

- The analog part is on a die in mature processes
- The digital part is embedded on a die in advanced processes

Fixed height for the analog ADC/DAC cores and second location of input peripherals

Fixed height for the analog peripheral well-defined width, limited to its necessary pad width

I/O pads not larger than the VIC's width

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FlexAudio Flexibility and Safety

Flexible Configuration – adding core blocks and peripherals if required

Resilience to Power Supply Noise – with embedded low noise linear regulator (nLR)

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FlexAudio Embedded Power Regulator
No other provider can do this

In a power management network (PMN), various sources and paths of power supply noise exist.

- Source 1 → Noise of Power Supply Source
- Source 2 → Noise of Linear Regulator
- Source 3 → Self-Pollution
- Source 4 → Backward Current Noise of Other Parts of the System

Having an embedded power regulator in the audio CODEC helps to increase resilience to power supply noise and optimize power consumption.

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FlexAudio Embedded Power Regulator
No other provider can do this

When Dolphin's CODEC is supplied directly by an embedded low noise Linear Regulator (nLR), **PSNP complies with PSNT2 → System performances guaranteed.**

nLR = low noise Linear Regulator
PMN = Power Management Network
PSNP = Power Supply Noise Profile
PSNT2 = Power Supply Noise Tolerance Template

Key Benefits:

1. Resilience to power supply noise
2. Reduce CODEC power consumption
3. Smart management of power consumption depending on end-user activity
4. Secure CODEC integration

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Bow & Chord Interface Topological Schematic
No other provider can do this

Bow Interface: a minimized number of pins

Die in advanced nodes (65 nm to 28 nm)

Area on a 40 nm die: 0.15 mm²

Area on a 0.18 μm die: 1.88 mm²

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FlexAudio Analysis of Risks: SNR/THD Drop and PuN

Possible issues during the integration of an audio CODEC:

- 1 Master clock jitter
- 2 Power supply noise
- 3 Audio data synchronization
- 4 Transition of modes

Diverse Configurations and Applications → Different Risks

p.12

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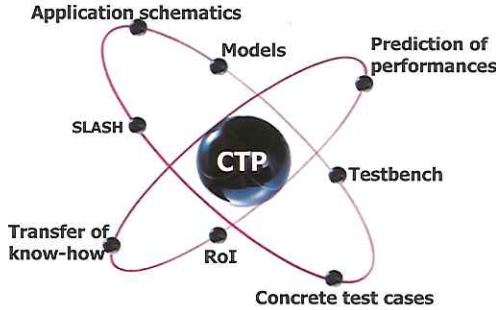
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DOLPHIN INTEGRATION

Dolphin's Transfer of Its Technical Know-How EMBLEM-CTP

EMBLEM-CTP (Case-study Tutorial Product) is:

- Transfer of know-how to SoC designers and Application Engineers through **generic case studies**
- Focused on **crucial hot spots**
- Needed at the frontier of IC and PCB design flows
- Built with **Dolphin's EDA point-solutions** integrating needed features and analyses



The diagram shows a central circle labeled 'CTP' with several points connected to it by lines: 'Application schematics', 'Models', 'Prediction of performances', 'Testbench', 'Concrete test cases', 'RoI', and 'Transfer of know-how'. A dashed line labeled 'SLASH' connects 'Application schematics' and 'Models'.

p.13

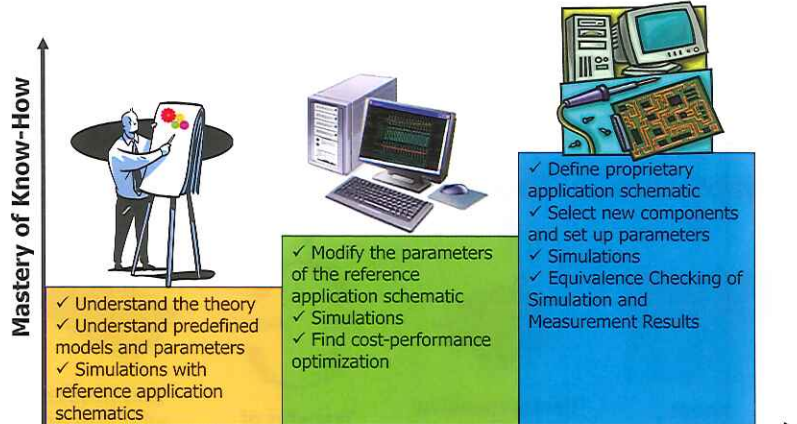
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DOLPHIN INTEGRATION

EMBLEM-CTP: A Step-by-step Process for an Efficient Transfer of Know-How



The diagram shows a vertical axis labeled 'Mastery of Know-How' and a horizontal axis labeled 'Steps of Know-How Acquisition'. Three colored boxes represent the steps: yellow, green, and blue. Each box contains a list of tasks.

- Yellow Box:**
 - ✓ Understand the theory
 - ✓ Understand predefined models and parameters
 - ✓ Simulations with reference application schematics
- Green Box:**
 - ✓ Modify the parameters of the reference application schematic
 - ✓ Simulations
 - ✓ Find cost-performance optimization
- Blue Box:**
 - ✓ Define proprietary application schematic
 - ✓ Select new components and set up parameters
 - ✓ Simulations
 - ✓ Equivalence Checking of Simulation and Measurement Results

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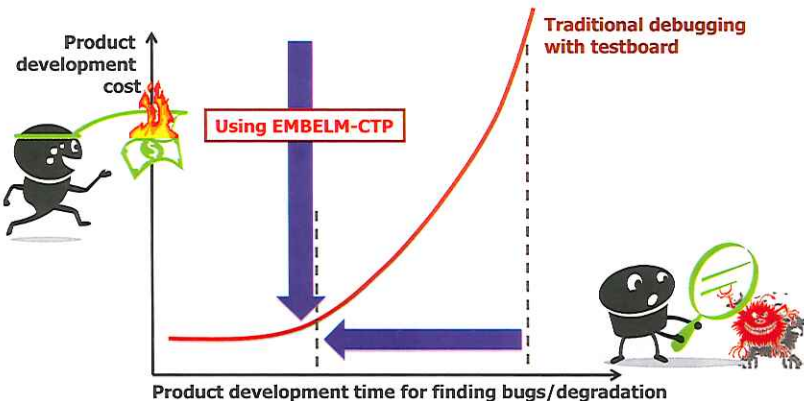
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DOLPHIN INTEGRATION

EMBLEM-CTP: Optimized Design and Production Efficiency

Early assessment of system performances for ensuring performance achievement, enhancing design productivity, reducing Time-to-Market and cutting R&D costs.



The graph shows 'Product development cost' on the y-axis and 'Product development time for finding bugs/degradation' on the x-axis. A red curve represents 'Traditional debugging with testboard', showing a sharp increase in cost as time increases. A blue arrow labeled 'Using EMBLEM-CTP' points to a lower, flatter curve, indicating reduced cost and time. A cartoon character is shown running towards the left, and another character is shown debugging a circuit board.

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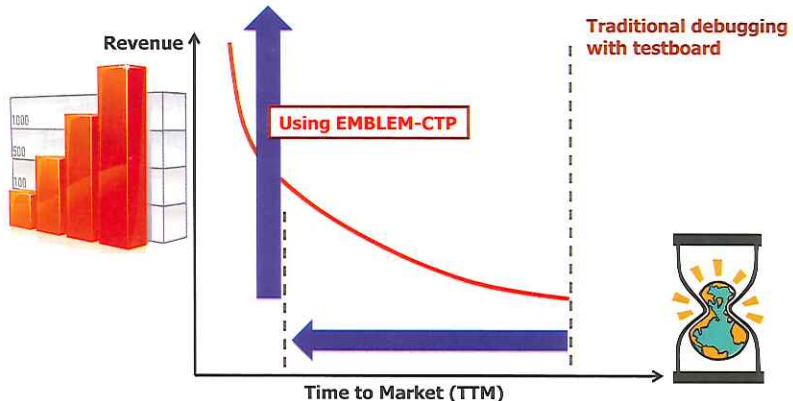
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DOLPHIN INTEGRATION

EMBLEM-CTP: Reduced Time to Market = Increased Revenue

Early assessment of system performances for ensuring performance achievement, enhancing design productivity, reducing Time-to-Market and cutting R&D costs.



The graph shows 'Revenue' on the y-axis and 'Time to Market (TTM)' on the x-axis. A red curve represents 'Traditional debugging with testboard', showing a sharp decrease in revenue as time increases. A blue arrow labeled 'Using EMBLEM-CTP' points to a higher, flatter curve, indicating increased revenue and time. A bar chart shows revenue increasing over time, and a cartoon character is shown running towards the left.

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DOLPHIN INTEGRATION

Mastery Needed for Safe Integration

Ingredients + Tools + Recipes = Good dish

- Ingredients:** Great Silicon IPs (IP 1, IP 2, IP 3)
- Tools:** Comprehensive EDA solutions (SLASH)
- Recipes:** Transfer of Technical Know-How (User, Dolphin)
- Good dish:** End-product with Turnkey Package

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DOLPHIN INTEGRATION

Helium 3 Novel Audio 95 dB CODEC

Beyond Bow interface advantages, Helium 3 has more innovations:

- On Headphone path: decoupling capacitance down to 47 μF from 220 μF without bass reduction for listener
- Novel Pop-up Noise reduction system
- True Ground on demand for Headphone outputs
- > 1 W output power for BTL with minimal silicon cost and minimal heat dissipation issue (MOSFET left on PCB)
or
> 2 W output power for BTL using TSMC BCD high voltage process

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DOLPHIN INTEGRATION

Helium 3 Novel Audio 95 dB CODEC

Power Consumption (mW)*

- 21.3
- 18.8
- 5.7

Helium 3 compared to its 2nd generation:

- **70% lower** power consumption
- Smaller area and higher performance
- Lower BoM cost for headphone output

* Measured path: DAC to Headphone

Second generation CODEC in 180 nm

Second generation CODEC with Bow interface 180 nm and 40 nm

Novel generation CODEC with Bow interface (Helium 3 architecture)

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DOLPHIN INTEGRATION

Dolphin's Offerings across all Process Nodes and with Bow & Chord Interfaces

Monolithic Architecture

Process Node	Architecture
180 nm	Helium 3
40 nm	Xenon
28 nm	Neodyme*

* Under development

Chipset Architecture

Bow & Chord Interfaces

180/150/130 nm

65/40/28* nm

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NOTE

This image shows a full page of blank, lined paper. It features approximately 20 evenly spaced horizontal grey lines across the entire width of the page, providing a guide for handwriting or typing. The background is a clean, solid white color.

TSMC 2012 Open Innovation Platform[®] Ecosystem Forum

The Trusted Technology and Capacity Provider



Solving ESD, EOS and Latch-Up Requirements
- For Analog Interfaces in Advanced CMOS
- For Automotive Applications in TSMC's BCD Platforms

SOFICS

ABSTRACT

IC designers continue to combine ever more analog features in advanced digital Systems-on-Chips (SoCs) like analog to digital and digital to analog conversion, sensor interfaces, audio/video handling. The design of these analog circuits is more complex and involves a lot of manual layout. TSMC supports its customers through Analog/Mixed Signal reference flows even for the most advanced CMOS nodes and through the availability of an ecosystem with several IP partners that can speed up design cycles and increase productivity. On top of this functional design complexity, circuit designers face challenges related to ESD protection: on-chip ESD concepts used in general purpose I/O's are not well suited for many analog designs because they introduce high parasitic capacitance, series resistance and leakage current.

On the other hand, similar problems exist in BCD platforms for automotive applications. The amount of electronic circuits in cars has been steadily increasing to an average of more than 50 ASICs per car. Not only the number of circuits in cars has been expanding. Also the quality requirements have been continuously increasing. While on-chip ESD requirements are being lowered in consumer electronics the specifications for automotive parts have only been increased. LIN/CAN interfaces for instance must pass stringent system level ESD stress (IEC 61000-4-2) of more than 6kV. This increased requirement strongly limits the options for ESD protection. Furthermore there are many non-ESD requirements that affect the selection of the most appropriate ESD concept: Electrical OverStress (EOS), Electromagnetic compatibility (EMC) and of course (transient) latch-up.

This presentation provides an overview of the typical issues designers face when they want to protect their circuits against Electrostatic Discharge. Through a set of case studies different on-chip ESD protection concepts which are available through the TSMC IP eco-system are compared.





ESD SOLUTIONS AT YOUR FINGERTIPS

BART KEPPENS, DIRECTOR TECHNICAL MARKETING

SOLVING ESD, EOS AND LATCH-UP REQUIREMENTS

- FOR ANALOG INTERFACES IN ADVANCED CMOS
- FOR AUTOMOTIVE APPLICATIONS IN TSMC'S BCD PLATFORMS

Outline

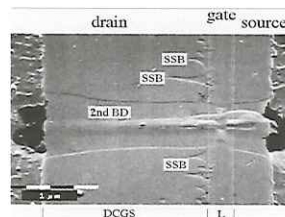
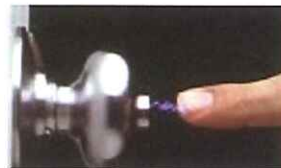
- **Introduction**
 - On-Chip ESD protection
- Protecting Analog Interfaces
- Protecting High Voltage applications
- Conclusions

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What is ESD? – Physical phenomenon

- What is Electrostatic Discharge ('ESD')?
 - The sudden discharge of a charged body
 - Short time (<1us)
 - Short rise time (<10ns)
 - High current levels (1-10A)
 - Tribo-electric and induced charging
- Importance of ESD for IC industry
 - Silicon melting, junction or gate breakdown
 - Industry quotes about ESD failures:
 - "Responsible for 20-30% of IC failures"
 - "25.8% of the products rejected"
 - "Estimated 8 to 33% of all product losses"

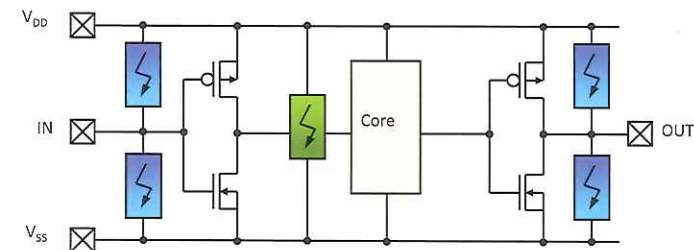


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Solution: on-chip ESD protection

- On-chip ESD protection
 - ESD clamp/diode devices at IO interfaces, power pads
 - Different concepts are used in the industry



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Outline

- Introduction
- **Protecting Analog Interfaces**
 - Analog I/O
 - Requirements
 - Case studies
- Protecting High Voltage applications
- Conclusions

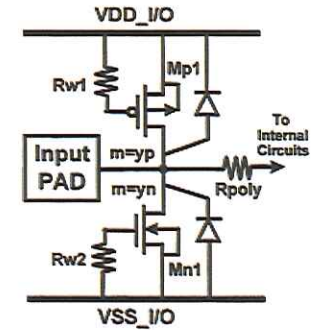


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GPIO ESD concept not suitable for Analog I/O

- Typical GPIO ESD protection concept
 - ESD robust output drivers
 - Large NMOS/PMOS transistors
 - Silicide blocked drains
 - Integrated diodes
 - Poly resistance between ESD and circuit
- Issues
 - Prevent high speed circuits
 - High leakage current
 - Large silicon area
 - High parasitic capacitance



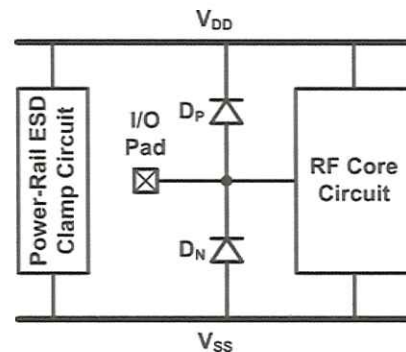
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Solution: Typical Analog I/O – diode based approach

- Traditional Analog I/O
 - Simple concept
 - Diode from Vss to Pad
 - Diode from Pad to Vdd
 - Needs efficient power clamp
 - Good characteristics
 - Low leakage
 - Low parasitic capacitance
 - Small area
 - **BUT: room for improvement**
 - Lowest capacitance???
 - Overvoltage tolerant???
 - Protection of sensitive nodes???



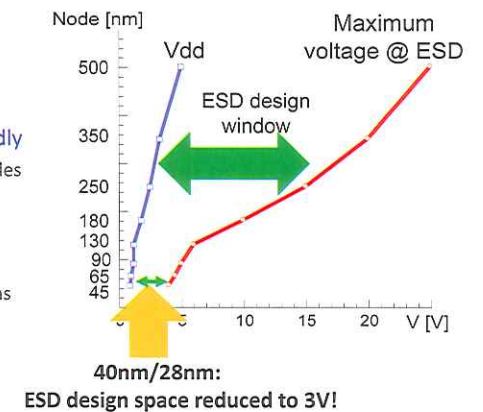
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Problem 1: Protecting sensitive nodes

- Decreasing solution space
 - Normal operation (VDD)
 - Slight decrease
 - Maximum voltage decreases rapidly
 - Transient breakdown of gate oxides
 - Burn-out of output drivers
 - Core failure voltage
 - Difference = ESD design window
 - Rapid reduction of design margins

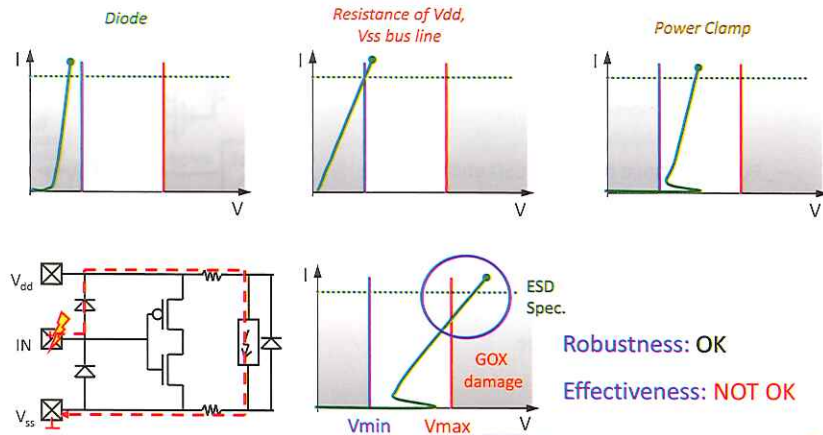


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'Dual diode' protection difficult in advanced CMOS

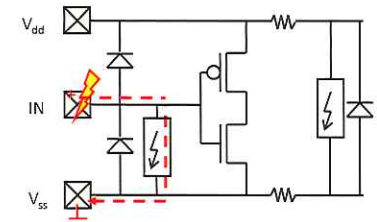


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Solution: Local I/O clamp reduces total voltage drop

- Local I/O clamp
 - Strongly reduce voltage drop during ESD
 - Many different device options
 - Place power clamp in the I/O !?
- Concerns?
 - Leakage current at I/O?
 - Parasitic capacitance at I/O?
 - Silicon footprint?
 - Latch-up immunity?

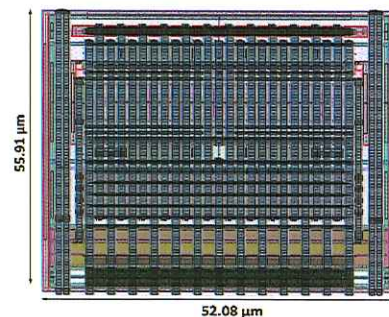
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Example: Local I/O clamp protects RF-IO, TSMC 90nm

- ESD protection for LNA IO
 - ESD: >2kV HBM
 - Latch-up immune
 - Low capacitive: <100fF
 - Low leakage: <0.1nA
 - Small area: <3000 μm^2
 - CUP: ESD under bond pad

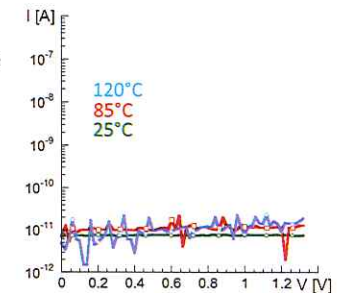
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Examples: Protecting low leakage analog interfaces

- Reduce ESD related leakage with proprietary ESD IP
 - Example: 1.2V TSMC 40nm
 - ESD protection for RF LNA circuit
 - Leakage ~20pA at 1.2V at high temperature
 - Example: 5V TSMC 180nm
 - ESD protection for overvoltage tolerant IO
 - Leakage ~10nA at 5V at high temperature
 - Example: 65nm ESD cells
 - All kinds of voltage domains
 - All kinds of interface types
 - Leakage ~20nA at high temperature

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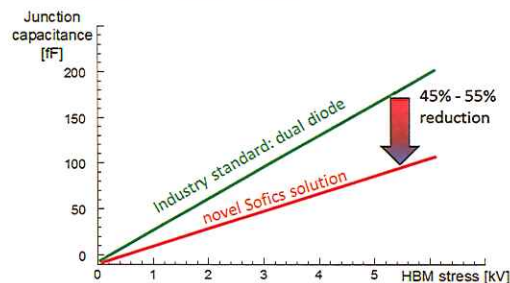
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Example: I/O ESD with low parasitic capacitance

- Innovation: Local ESD with ultra low parasitic capacitance

- Parasitic capacitance
- Silicon proven
 - 65nm: - 45%
 - 28nm: - 55%
- Reduce cap for same ESD
- Increase ESD for same cap



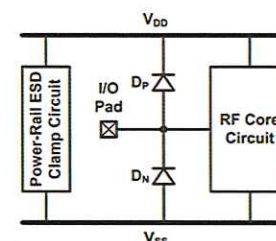
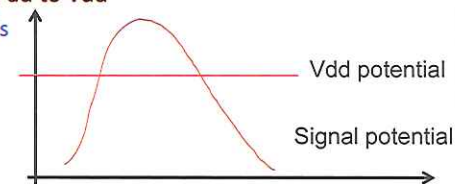
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Another issue with diodes: Signal voltage limitation

- Problems introduced by diode from Pad to Vdd

- Voltage level differences between ICs
- Shared communication line
- High speed interface
- Hot swap
- Back drive protection
- Inductive loads

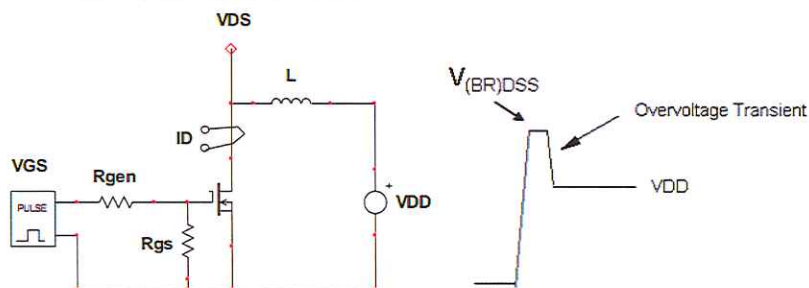


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Inductive switching creates voltage over shoot

- Unclamped inductive switching
 - Voltage overshoot on drain-source
 - 'Diode up' not always tolerated



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Examples: Protect high voltage capable/tolerant IOs

- Sofics proprietary clamps for high voltage / overvoltage tolerant interfaces
 - 3.3V based on 1.8V – SD/SIM card 40nm + 28nm
 - 5V based on 3.3V – HDMI 130nm
 - 5V tolerant IO's – TCON (LCD panel) 180nm + 130nm
 - 5V tolerant IO's based on 3.3V – HDMI 130nm
 - 15V flash protection 65nm
 - 15V based on 5V – Battery charger 0.25um
 - NEW:** 4V, 5V, 6V and even >10V protection 28nm

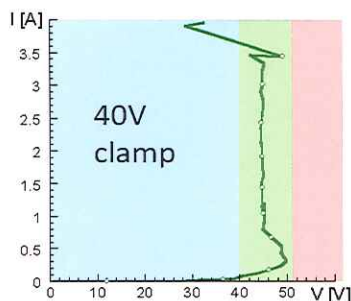


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TSMC 0.25-micron BCD gen I – ESD solution for LIN

- Passing severe EOS specifications
 - IEC 61000-4-5
 - Lightning specification used for EOS testing
 - ISO 7637-2
 - 'load dump' pulse (#5)
- Scaleable Sofics solutions: V_{t1} , V_h , I_{t2}
 - Physical limit: IO breakdown voltage
 - Example for 0.25um BCD 40V
 - NMOS breakdown ~52V
 - ISO 7637-2 pulse 5: 48V achieved



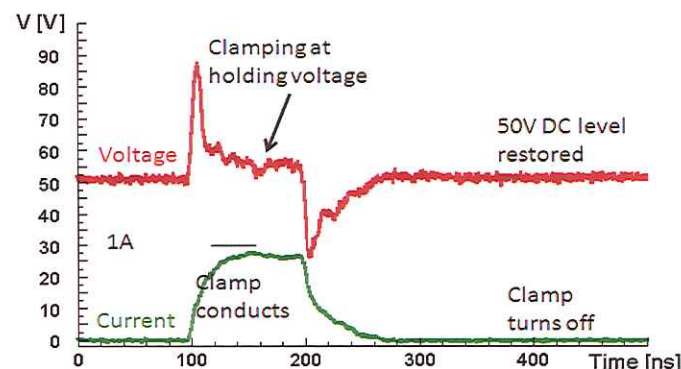
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TSMC 0.25-micron BCD gen I – ESD solution for LIN

- 40V clamp passes severe transient latch-up requirements
 - 50V DC Bias + 1A ESD pulse
 - Powered state: no clamping/latching after transient has passed



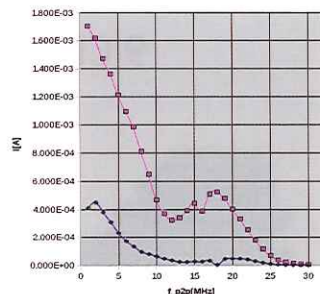
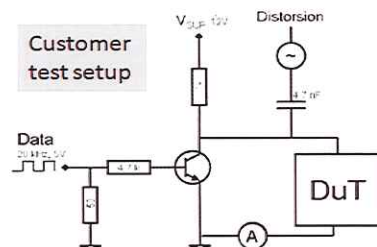
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TSMC 0.25-micron BCD gen I – ESD solution for LIN

- Passing severe EMC specifications
 - Example: experienced IC maker for automotive applications
 - PowerQubic assessment for IEC 62132 DPI



- Result: Sofics PowerQubic devices tested
 "...better performance in EMC tests than the ESD structure we used so far"

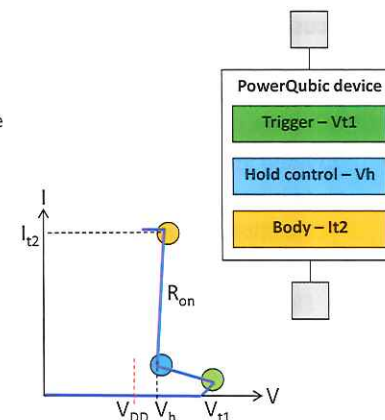
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Protect HV interfaces with Sofics' tunable clamps

- Tunable trigger voltage V_{t1}
 - External trigger circuit
 - Separate and interchangeable
 - Well established TakeCharge technique
- Tunable holding voltage V_h
 - Holding circuit variations
 - By layout and/or design
 - Novel approaches
- Tunable performance I_{t2} , R_{on}
 - Clamp size variation
 - Different clamp bodies



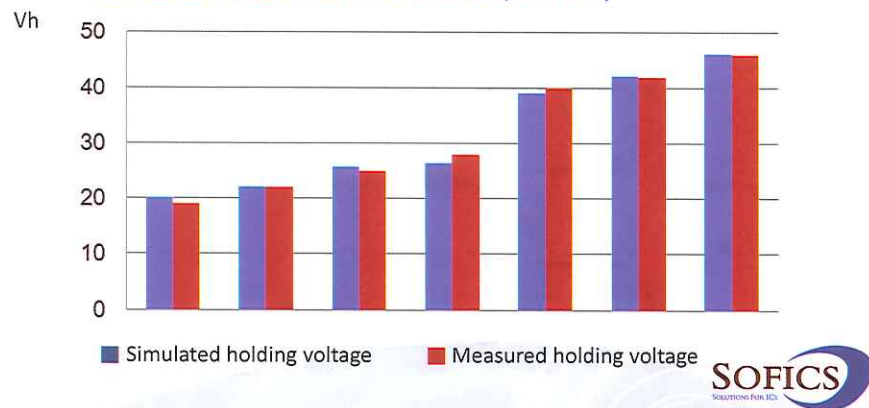
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Predictable behavior: Simulate V_h before tape out

- Predictable behavior
 - Independence of triggering, clamping and failure levels
 - Proven effectiveness, robustness and latch-up immunity



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Outline

- Introduction
- Protecting Analog Interfaces
- Protecting High Voltage applications
- Conclusions**



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Conclusion: On-chip ESD clamps available

- Focus on key challenge for IC applications: on-chip ESD protection
 - Important reliability aspect
 - Destruction of semiconductor devices
 - Millions of dollars in real losses each year
- Provided an overview of the requirements for on-chip ESD protection
 - Focus on analog and high voltage applications
 - Traditional solutions cannot handle all requirements
- Presented Sofics ESD solutions
 - Flexible IP portfolio to address various requirements
 - Technical and financial benefits
 - Verified and available on many TSMC platforms

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Sofics on-chip ESD clamps protect a broad range of applications and technologies

1500+ products

rely on Sofics ESD protection

9 CMOS generations

CMOS 0.5um down to 28nm

25+ TSMC customers

include Sofics ESD IP for beyond standard IOs

50+ customers

protect chip interfaces with Sofics ESD



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TSMC – Sofics cooperation



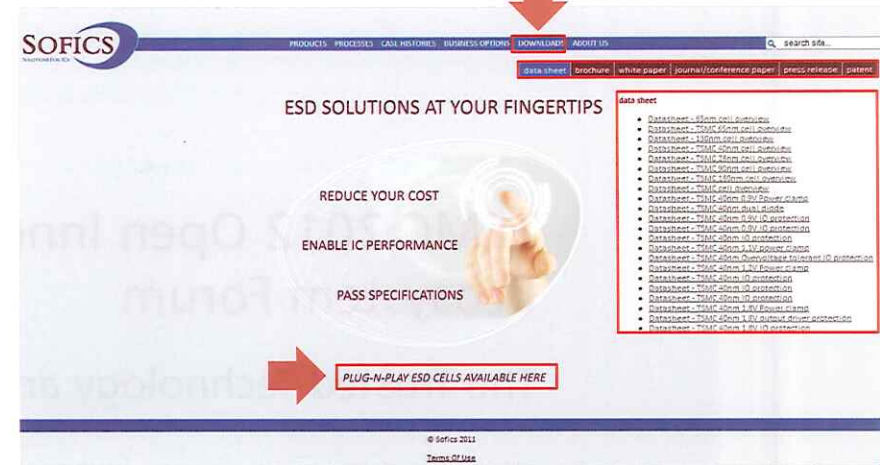
- History
 - 2008: Design Center Alliance partner
 - 2010: TSMC Licenses Sofics PowerQubic™ Technology for 0.25um BCD Process
 - 2010: IP Alliance partner
 - 2011: First libraries approved and online
- Sofics serves 25+ TSMC customers
 - Sofics solutions complement foundry clamps
 - TakeCharge: any CMOS down to 28nm
 - 0.18-micron 0.13-micron 90nm
 - 65nm 40nm 28nm
 - PowerQubic: from 0.35-micron to 0.18-micron BCD
 - 0.35-micron High voltage
 - 0.25-micron BCD & 0.18-micron BCD Gen I – solutions available
 - 0.25-micron & 0.18-micron BCD Gen II – ongoing project



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Sofics website – downloads

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 - USA: DSM Silicon Solutions // Design Rivers
 - Israël: ETesiAN Semiconductor
 - S-Korea: Acetronix
 - Taiwan: Maojet
 - Japan: CTC // IPN
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www.sofics.com

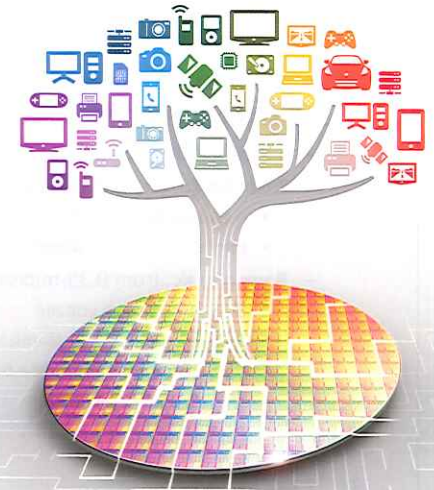


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Enabling Design with Advanced Node Design IP for TSMC

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ABSTRACT

In this presentation we will explore the Cadence 20nm Design IP roadmap including the capabilities and innovations that have been required to make the IP available in 20nm. We will look at multiple IP areas including our Industry leading DDR PHY's that delivers both low power and high performance operation and our high performance SeDes designs.

As part of the presentation we will discuss the methodology used, and experiences in designing for 20nm.

Finally with integration now a key consideration of successful adoption of IP, we will close by looking at the enablement infrastructure that is needed to ensure success at 20nm including Verification IP and System Integration IP.

Enabling design with advanced node design IP for TSMC

Amjad Qureshi, Senior Group Director R&D, SoC Realization Group

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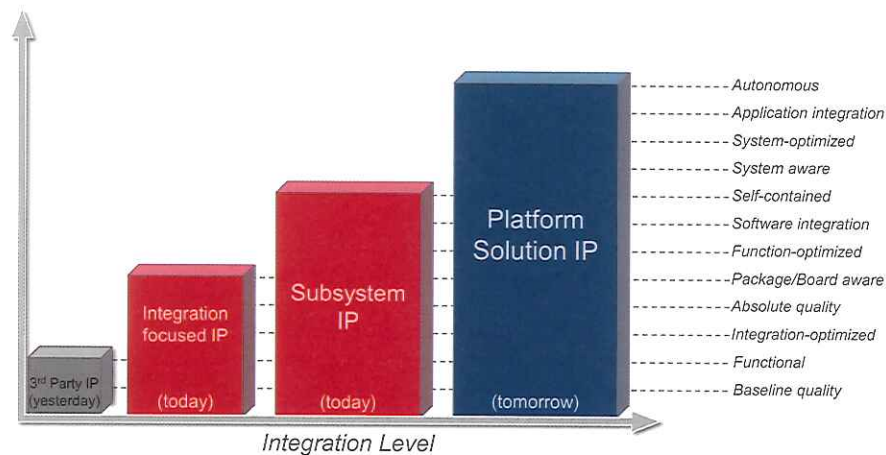
Agenda

1. Design enablement needs at advanced nodes
2. Collaboration with TSMC at advanced nodes
3. Example of design enablement with DDR IP
4. IP portfolio and roadmap

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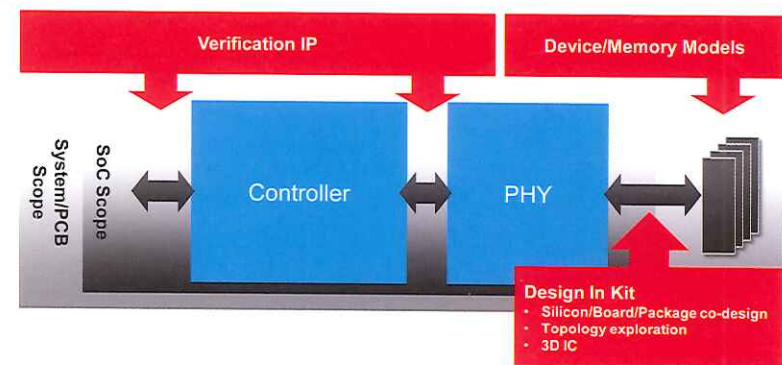
Advanced node success requires a broader IP definition



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What do we mean by “Integration Focused IP?”



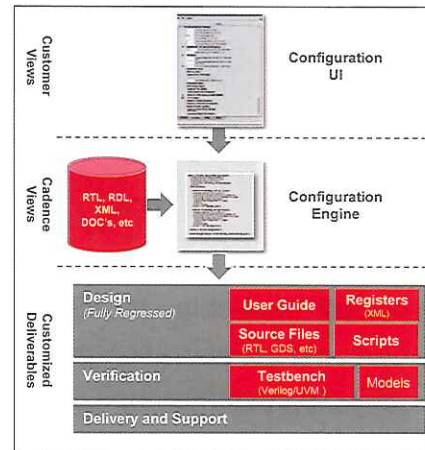
- Fully-integrated solutions are fully
- Extensive verification using verification IP and memory models
- Fully characterized test chips across process nodes
- System design with silicon, board and package for subsystem IP sent for certification and industry interoperability testing

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Require approach to design that is application aware as well as process aware

- Unique approach ensures the optimal implementation for design
 - Proven success with the thousand of cores delivered
- Allows architects to specify the exact requirements for their design
 - Get what is needed - not more and not less
- Deliverables customized for the target design
 - Includes full support for advanced node methodologies



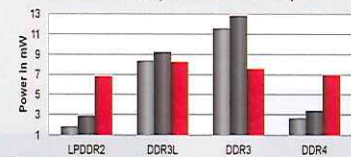
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Differentiation is still critical

POWER

28 HPM Power Dissipation at Max Protocol Speed



- ✓ 6 power saving modes for DDR controller
- ✓ 75mW Read/103mW Write LPDDR3 32bit PHY*
- ✓ 7.5mW/Gbps/lane for PCIe gen 3 PHY*

PERFORMANCE

Difficult traffic, Cadence reordering engine off: 44 percent bandwidth

Same traffic, Cadence reordering engine on: 76 percent bandwidth

- ✓ Up to 30% bandwidth gain with DDR controller
- ✓ DDR 4 PHY at 2400 scaling to 3200*
- ✓ First to market w x16 PCI-gen 3

AREA



- ✓ Only ~ 3 mm^2 in area LPDDR3 32bit PHY*

ROBUSTNESS



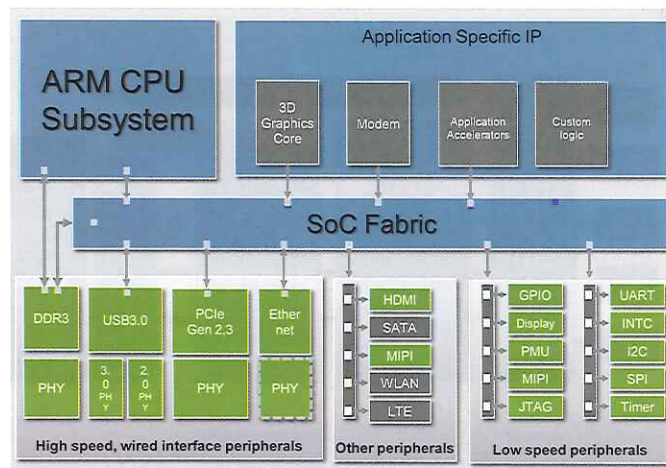
- ✓ 28nm test chips with characterization data
- ✓ 20nm test chips in design
- ✓ Pre- and Post silicon Interoperability testing

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* TSMC 28nm

The need for proven IP



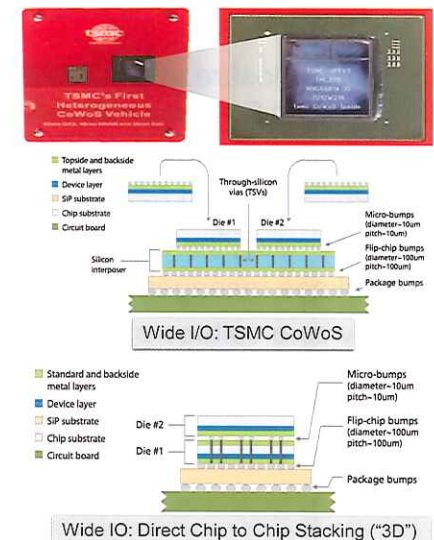
- Tape out reference SoC every 3 months with customer configurations
- Drive software development and build design-in kits
- Enable customer to evaluate the quality of our IP

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Cadence and TSMC have been early with leading edge technology

- First to market with design IP for new interface standards
 - WideIO
 - DDR4
 - LPDDR3
 - PCIe Gen3
- Leading the move to new implementation technologies
 - 20nm
 - CoWoS
 - 3D IC
- Adopting advanced digital and mixed signal methodologies for advanced nodes

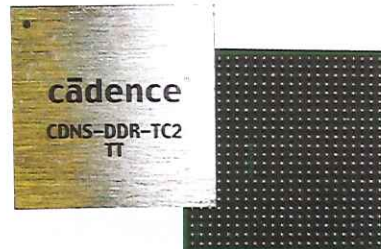


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Collaboration is the key to success

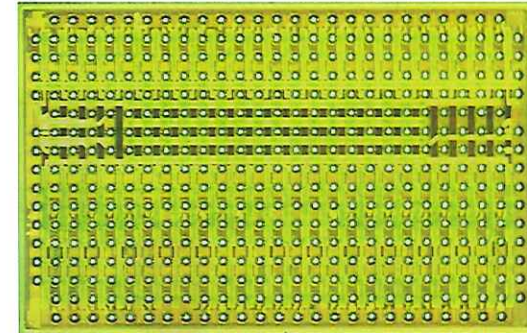
- Advanced node design is challenging and a reason designers turn to IP
- As an IP designer, collaboration with the foundry is critical to success
- TSMC is a key collaborator for us providing
 - Early access to process information
 - Process expertise
 - Test chip and shuttle support



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Experiences with TSMC advanced nodes



- Multiple test chips for TSMC 28HP and 28HPM
- Ongoing collaboration around TSMC 28LP and 20SOC
- Multiple customer tape outs in TSMC 28HP and 28HPM

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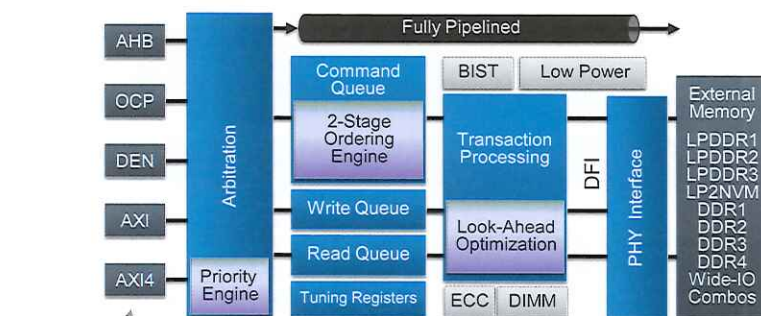
Key challenges and learning's dealing with advanced node design enablement

- Timing closure at all corners and OCV conditions
 - Meeting Setup and Hold at 0,125 and -40C
- Orientations and layout schemes
- Metal stack and ESD rules
- Noise and jitter tolerance
- Leakage management with multiple power grids
- Low core voltage operation

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Highly configurable IP ensures a match for every design



Multiple Bus Type Support

Busses are configurable for type, width, FIFO arrangement, synchronicity, and more. Once configured, programming controls even more behavior.

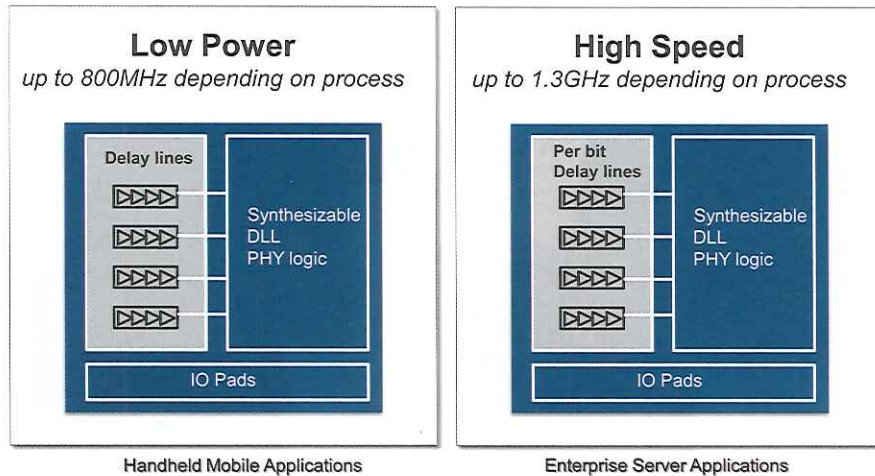
Configurability

Most things in the controller are configurable or resizable to match the exact system needs. If a feature is not needed, it is entirely removed from the RTL, scripts, and docs.

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PHY “Slice” architecture delivers performance, flexibility, and ease of integration



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PHY architecture enables implementation across a range of TSMC technologies

- Supports DDR4/DDR3/DDR3L/DDR2/DDR1/LPDDR3/ LPDDR2/LPDDR1
- Industry standard DFI 2.1 and 3.0 memory controller interface
- Integrated I/O pads with data retention mode, integrated DLL/PLL
- DIMM support with leveling
- Register interface for PHY programming
- Full scan with external and internal loopback modules

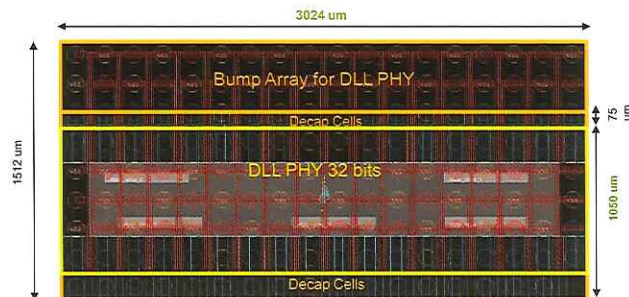
Programmable settings

- DLL/PLL
- I/O settings
- DFT loopback control
- Gate tuning
- Read/write leveling
- Power mode setting
- DFS support via DFI

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Implementation methodology for 28HPM 32 bit DLL PHY supporting LPDDR2/LPDDR3



- Hardened byte based data slices
- Hardened address controller slice logic
- 2 I/O row implementation with dedicated decaps
- 151 actual bump pitch with 1P8LM
- Flip chip package

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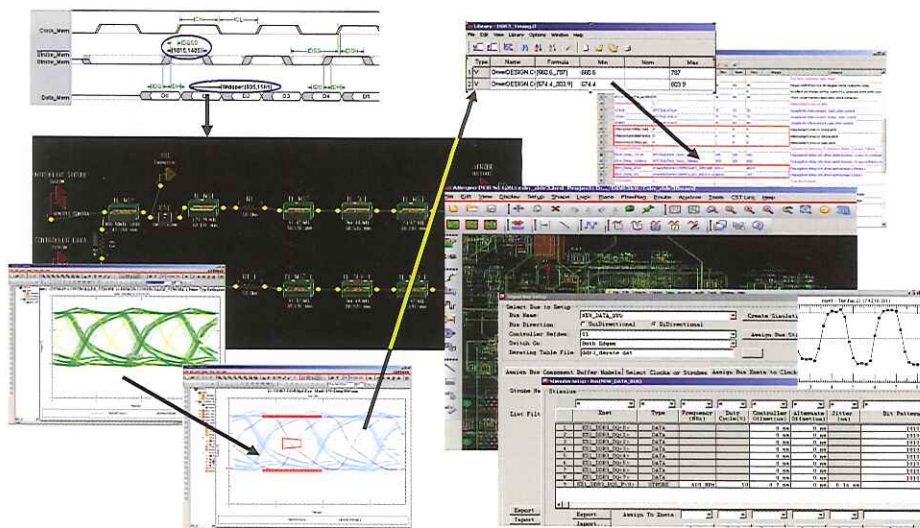
IP deliverables support TSMC methodologies for predictable advanced-node design

- Synthesizable full PHY RTL
- User guides and documentation
- Synthesis and STA scripts
- SDC constraints
- PHY layout guidelines
- Basic testbench
- DFI monitor
- Register configuration utility
- DDR PHY Interface (DFI) compliance
- Hard/Firm PHY (TSMC 40nm and 28nm) [lib,lef,gds,v,ibis]**
- Custom PHY hardening options

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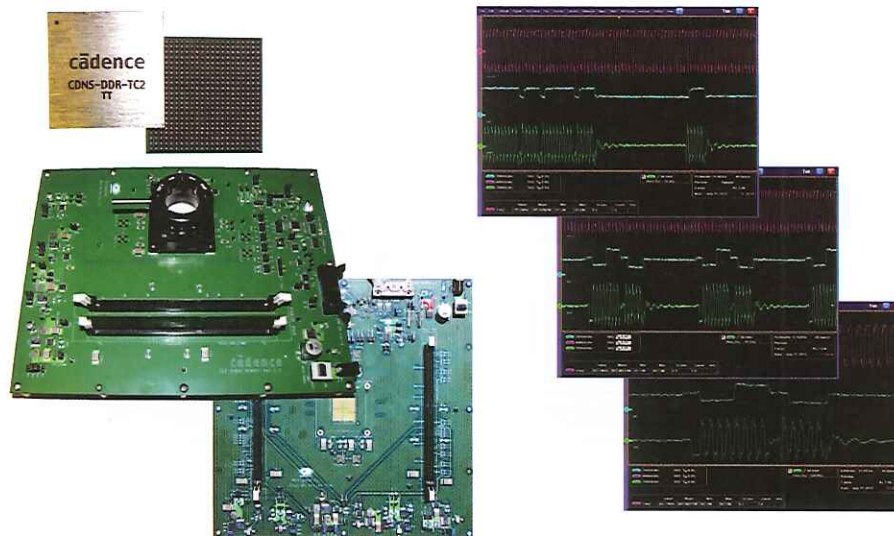
System Integration IP enabling true silicon/package/board co-design



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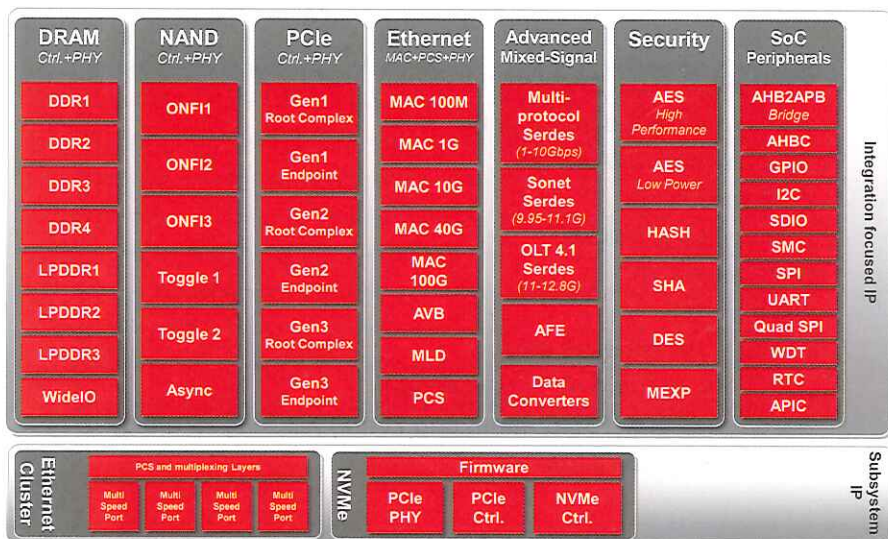
Extensive post silicon validation for TSMC's advanced nodes



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Cadence's rapidly expanding IP portfolio



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Kilopass Roadmap for Advanced TSMC Processes

Kilopass

ABSTRACT

From its inception at 180nm, the first process node where gate oxide breakdown (BVox) voltage fell below junction breakdown (BVj) voltage, one-time programmable (OTP) anti-fuse technology has provided a tamper-resistant and reliable non-volatile memory solution in standard logic CMOS. As process technology continued to scale downward, the anti-fuse program voltage used to breakdown the gate oxide decreases with transistor dimensions and the oxide thickness. At the same time, OTP security, reliability, and storage density improves with scaling. With OTP product reliability qualified on 28nm HKMG and cell functionality demonstrated for 20nm, Kilopass' OTP technology offers a highly scalable and manufacturable embedded NVMs solution at advanced process nodes with no technology roadblocks on the horizon even with the migration to FinFet and other 3D device architectures. This presentation describes Kilopass' OTP roadmap for all variants of TSMC's advanced process nodes.





Kilopass Roadmap for Advanced TSMC Processes

Outline

- About Kilopass Technology
- Overview of Kilopass OTP cell technology
- Kilopass OTP memory on high-k metal gate process
- Kilopass OTP technology scaling to 20nm and beyond
- OTP applications and Kilopass technology roadmap
- Summary

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Kilopass Corporate Overview

Logic NVM Innovator

- Kilopass founded 2001, standard CMOS possible, Gox breakdown < BV_j
- Conceived at the right time, when 0.18μm came to market

Proven & Patented Embedded NVM in CMOS

- 58 patents granted/pending, including fundamental patents on 1T, 2T, and 3.5T anti-fuse
- 0.18μm to 40nm qualified and in production; 1st to demonstrate reliability in 28HKMG; T/O-ed 20G, 20SOC

Broadly Adopted

- 150+ customers
- 400+ design ins
- 2 billion+ units shipped

Key Markets

- Analog: audio tuners, clock chips, PMU, LED lighting
- Automotive: DSP, I/O connectivity, micro sensor systems
- Mobility: PA, RF transceiver, baseband, DDI, CIS
- Consumer: media & app processors, PC multimedia

Key Usages

- Small capacity (< 256Kb): Configuration, yield recovery, security keys, code patching of ROM
- Large capacity (> 512Kb) : Code storage

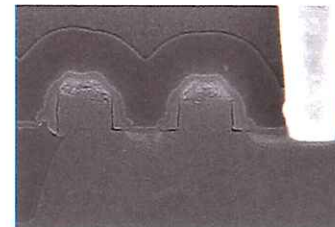
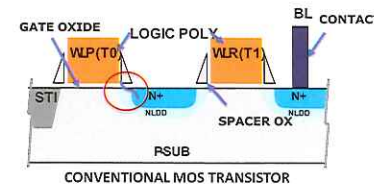
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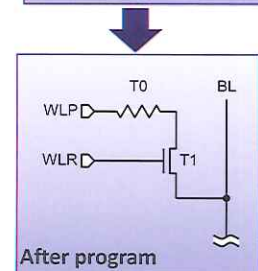
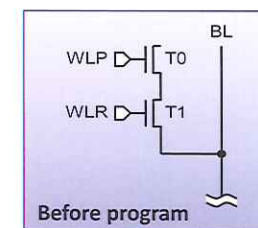


2T Bitcell – Cell Design

Cell Cross Section



XPM Cell Schematic

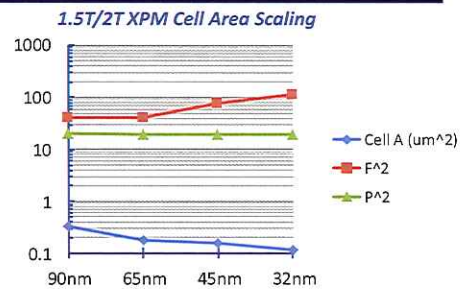
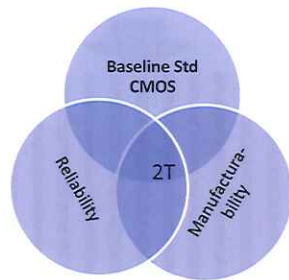


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4



The eOTP Technology for Manufacturability & Reliability



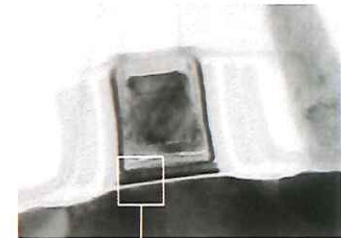
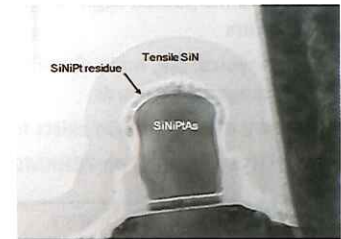
- 1 Standard NMOS –no special masks, overlay tolerance or process control
- 2 Follows DFM design rules
- 3 Scales with poly and active half pitches (P²)
- 4 Separate program and read transistors enables gates ensures independent optimization of program, program disturb and parasitic leakages.

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Excellent Manufacturability, Scalability, and Reliability on HKMG

- Cell array uses foundry standard nMOSFETs only
- No non-critical mask features inside memory array
- Fully compliant to DFM rules and independent of HKMG integration scheme
 - HKMG First
 - HK First/Metal Last
 - HKMG Last
- Excellent reliability demonstrated on 28nm and scalability to 20nm and beyond, planar or 3D



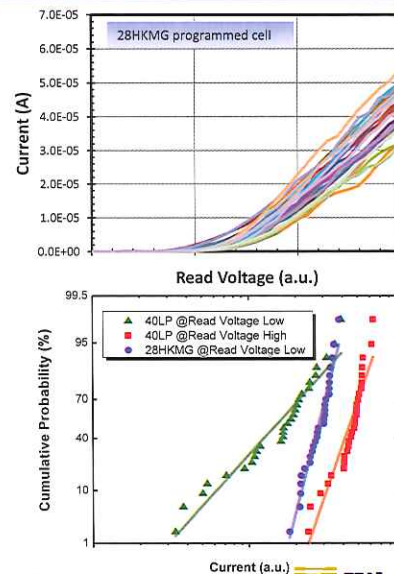
(James, ASMC 2012)

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28HKMG OTP Shows Even Better Programmed Cell Current

- 28HKMG gives much tighter distribution on both read current and 'turn-on' voltage, compared to 40LP
 - Antifuse link of poly gate is formed by breakdown-induced epitaxial growth. Relative small conductivity and large local variability contribute to breakdown hardness and therefore a larger spread of cell read current.
 - Antifuse link of HKMG is formed from metallic ion migration. Due to its high conductance, the traditional soft breakdown is hardly observed at typical OTP program conditions.

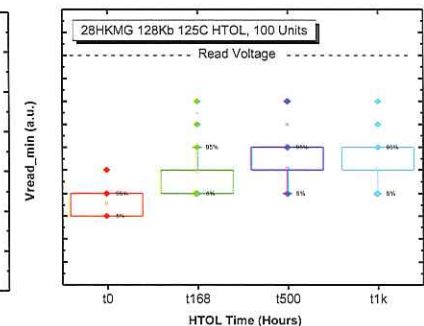
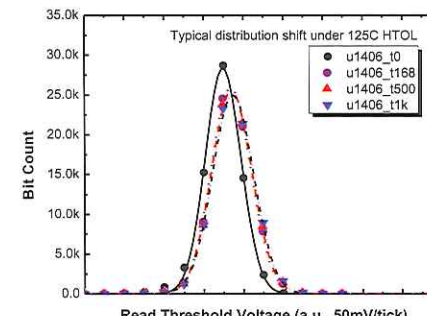


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28HKMG OTP Passed 1Khr HTOL for Both Ext- and CP-Vpp

- No program failure observed on qualification lot
- All units passed High Temperature Operating Life (HTOL) test at 168, 500, and 1K hours
- For a typical die, main distribution shift is about 20~40mV at 168 and stays unchanged afterwards
- Excellent HTOL reliability similar to that of Poly/SiON process

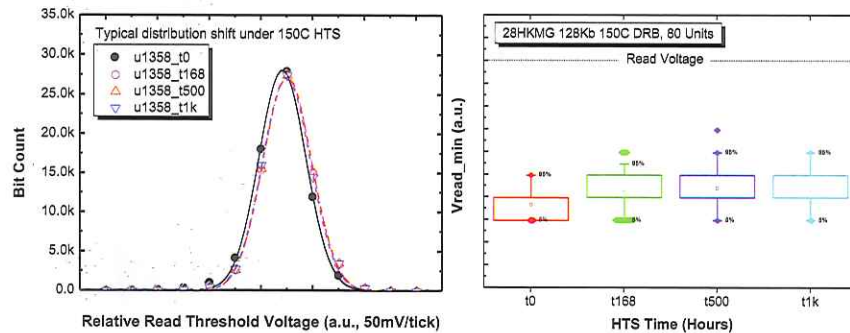


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28HKMG OTP Passed 1Khr HTSL for Both Ext- and CP-Vpp

- All 80 units passed High Temperature Storage Life (HTSL) test at 168, 500, and 1K hours
- For a typical die, main distribution shift is about 10~30mV at 168Hrs and stays unchanged afterwards
- 150mV of read margin exists for the few worst units at 1000 hours
- OTP HTS reliability on 28HKMG can be even better than that of Poly/SiON



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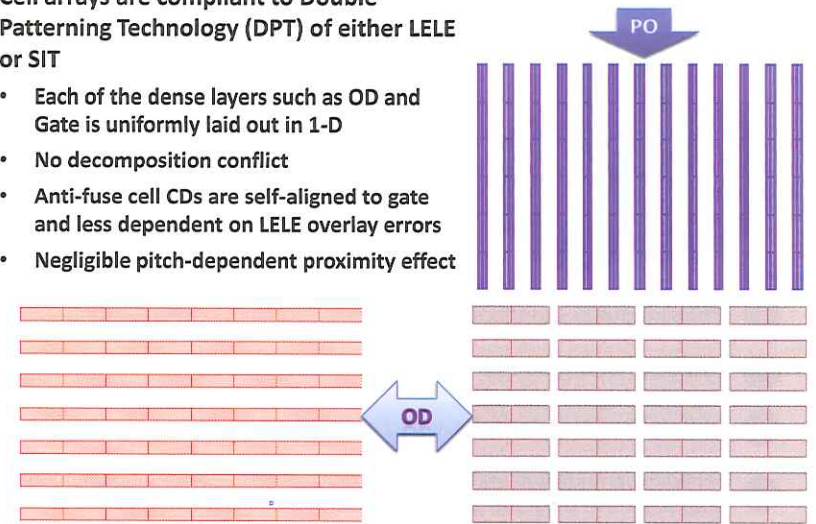
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Kilopass OTP Scales Very Well to 20nm and Beyond

Cell arrays are compliant to Double Patterning Technology (DPT) of either LELE or SIT

- Each of the dense layers such as OD and Gate is uniformly laid out in 1-D
- No decomposition conflict
- Anti-fuse cell CDs are self-aligned to gate and less dependent on LELE overlay errors
- Negligible pitch-dependent proximity effect



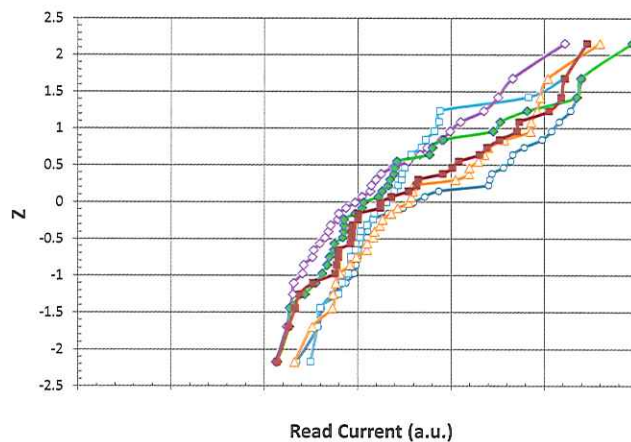
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Kilopass Achieved Excellent Cell Results on 20nm Silicon

- Programmed cell current across cell dimensional splits
 - W=100~140nm, L=26~30nm
 - Demonstrated excellent manufacturability and process control tolerance



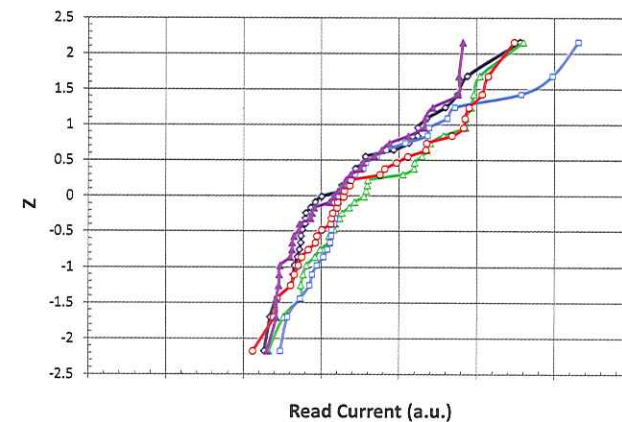
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Kilopass Achieved Excellent Cell Results on 20nm Silicon

- Good programmed cell current under varying program conditions
 - Vpp±100mV and w/ different program current controls
 - Charge pump and periphery reliability will be better than 28nm due to a lower program Vpp



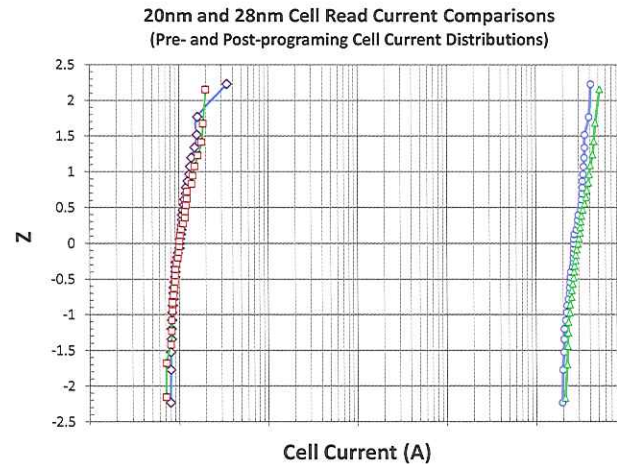
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Kilopass Achieved Excellent Cell Results on 20nm Silicon

- Similar to 28HKMG, OTP on 20nm can achieve an operating window of >3 decades between programmed and un-programmed cells



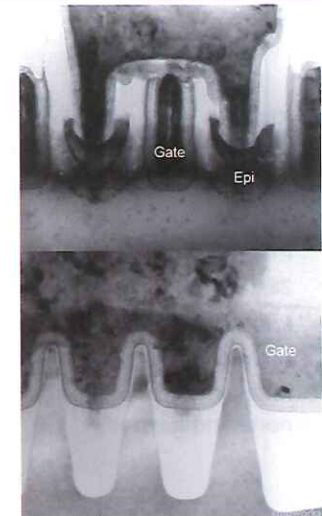
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No Major Challenges Seen for Anti-fuse Design on 1x FinFET

- FinFET technology itself is indeed challenging enough simply due to 3D topology
- Kilopass' 2T anti-fuse cell does not add any additional requirement on top of standard LV n-FETs
 - Quantization of fins – 1-fin cell
 - Gate dielectric – uniform and self-aligned
 - Gate definition – DPT or EUV
 - S/D and extension doping – same requirements as logic
 - Fin contact – potentially cell width limiting
 - Body punch-thru – low array inhibit voltage of $\sim V_{pp}/3$



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eNVM Applications on TSMC Advanced Technology Nodes

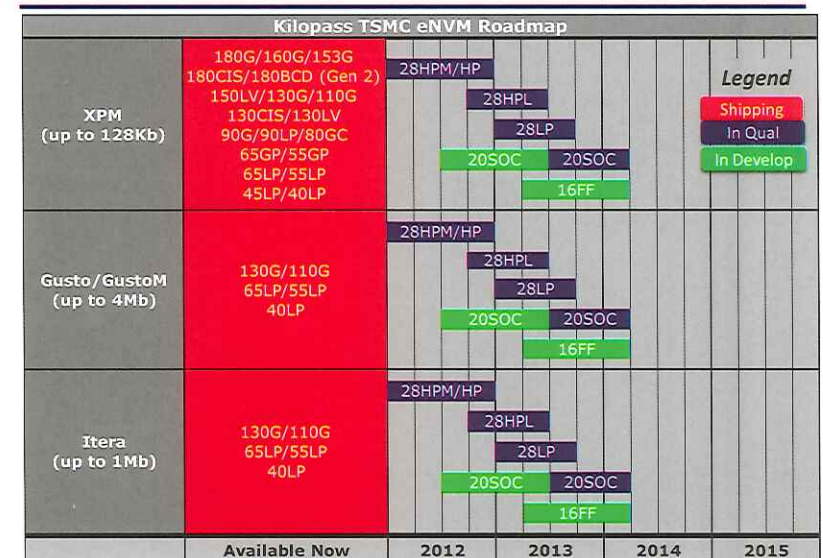
Technology Node	Pervasive Markets	Density	Key Usages	Benefit
28HPM	Baseband, Application Processors, Media Processors, SSD controllers	16Kb – 128Kb	Configuration, ROM patching, Security	•Security •Field update flexibility •Low Cost -> small area, low power
28HP	Computing, Network Processors	4Kb – 64Kb	Configuration, Yield Recovery, Security	•Security •Customization
28HPL	Media Processors, Application Processors, Multi-com	8Kb – 1Mb	Configuration, ROM patching, Security, Code Storage	•Reduction of BOM •Field update flexibility •Security
28LP	Low cost consumer Application Processors, Media Processors, Wireless Connectivity, SSD controllers	32Kb – 4Mb	Configuration, ROM patching, Code Storage, Security	•Reduction of BOM •Field update flexibility •Security
20SOC	Computing, Network processors, Baseband, Application Processors	4Kb – 128Kb	Configuration, yield recovery, Security	•Security •Field update flexibility •Low Cost -> small area, low power

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Kilopass eNVM Roadmap



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Summary

- Kilopass is a leader in embedded OTP memory and offers comprehensive solutions for advanced TSMC processes from 180nm to 28nm
- Kilopass' anti-fuse OTP memory works very well on HKMG processes
- 28HKMG OTP memories passed both HTOL and HTSL qualification
- From close collaboration with TSMC, Kilopass' 20nm OTP technology achieved excellent performance and manufacturability
- Kilopass' technology continues follow CMOS scaling trend to 1x node and beyond

NOTE

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Using Latest-Generation DDR4, LPDDR3 and Wide-IO DRAM Devices with Chips in TSMC's Advanced 28nm and 20nm Processes

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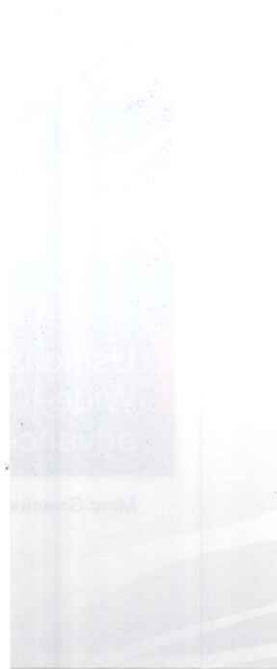
ABSTRACT

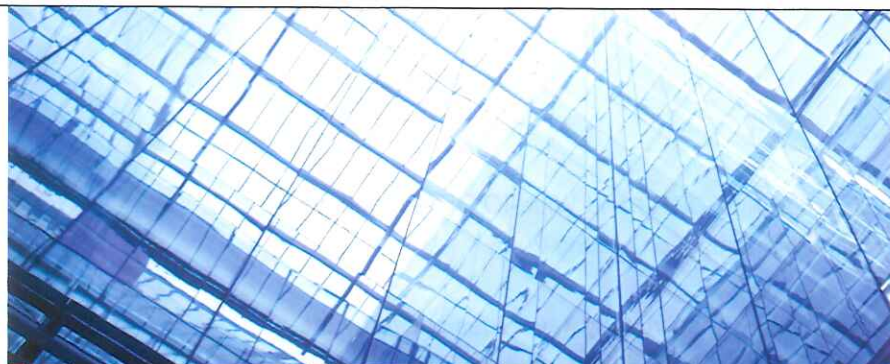
There has been significant progress on standards for high-speed DDR devices like DDR4, LPDDR3 and Wide-IO DRAM, and we may find these DDR devices in next-generation products as early as 2013 with mainstream adoption around 2015.

This presentation gives a brief introduction to each new technology and then discusses how to solve the key issues posed by the DDR devices using TSMC advanced technologies:

- How to reach high speeds of DDR4 like DDR4-2400 (2.4Gbit per pin) in TSMC28HP and TSMC28HPM
- How to reach low-power goals of LPDDR2 and LPDDR3 in TSMC28HPM
- How to build DDR interfaces in TSMC20SOC
- Using TSMC CoWoS™ technology to connect to Wide I/O DRAM

This presentation will discuss the desirable features of both controllers and physical (PHY) interfaces for these technologies, and present results seen on Cadence's Hard PHY testchips produced in TSMC 28nm process.





Using latest-generation DDR4, LPDDR3 and Wide-IO DRAM devices with chips in TSMC's advanced 28nm and 20nm processes

Marc Greenberg, Director, Product Marketing

mgreenberg@cadence.com

cadence

What is DRAM?

- Dynamic RAM used for temporary storage of data
- Usually the most cost-effective form of RAM
- Two kinds:

Embedded DRAM	Off-Chip DRAM
On the same die as logic	On a different die
Manufactured on logic process	Manufactured on DRAM process
Faster	Slower
Less capacity (MBytes)	More capacity (MBytes-GBytes)
Typically more cost per bit	Typically less cost per bit

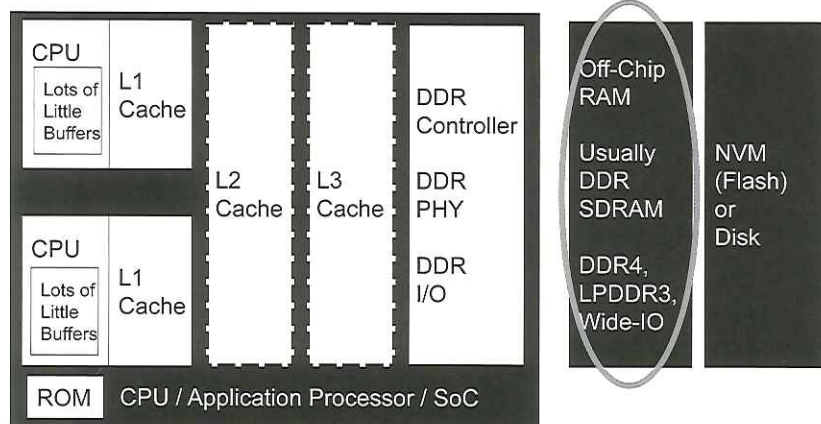
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How is DRAM Used Today?

Lower cost per bit and longer access time

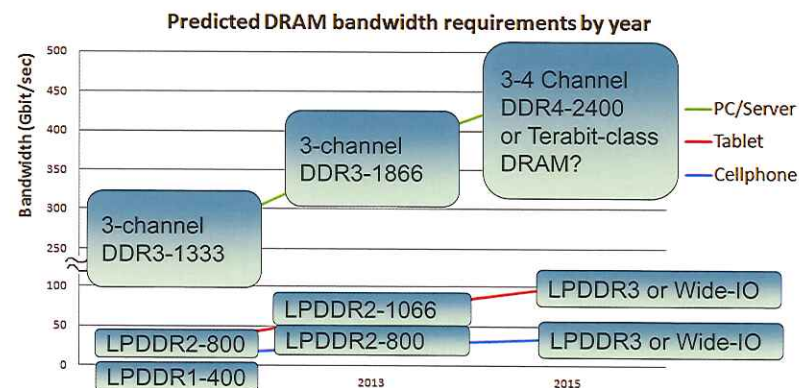


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Future DRAM Bandwidth Prediction



4

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DDR4: What Is It?

- Random Access Memory (RAM) chips used in computers, servers and consumer products
- Successor to Double-Data-Rate Synchronous Dynamic RAM (DDR SDRAM) - DDR1, DDR2, DDR3
- Unreleased* JEDEC standard several years in the making
- Collaborative standard developed by DDR4 users and manufacturers
- Predicted to be high volume DRAM in 2015**

*Unreleased as of presentation creation date in August 2012

** Cadence prediction

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DDR4: Why Do We Need It?

- Advances in PCs and servers demand more memory and higher memory bandwidth
- Demand for DRAM power reduction is universal
- Compared to DDR3, DDR4 is:
 - **Faster:** Up to 3.2Gbit/s gives more bandwidth, or fewer package pins needed for the same bandwidth
 - **More Mbytes:** Standard allows up to 16Gbit devices
 - **Less Power** per bit: Predicted power reduction up to 40% per bit
 - **Cheaper** (maybe): It is predicted that memory manufacturers will use their most advanced process nodes for DDR4 enabling DDR4 to become cheaper than DDR3 on a per-bit basis starting in the 2015 timeframe

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What's Needed in the DDR4 Ecosystem

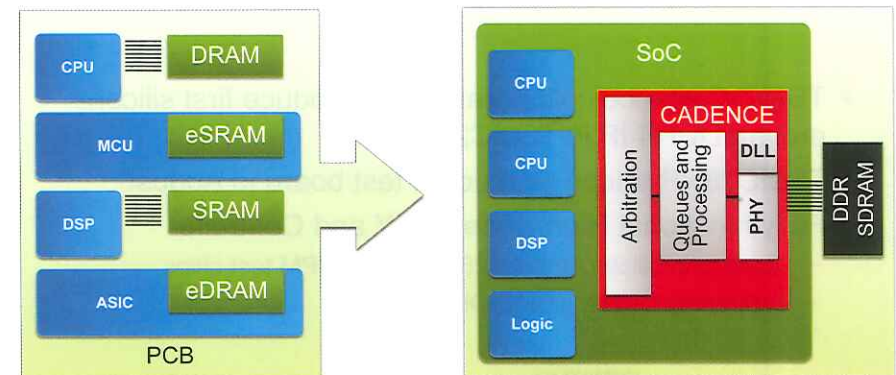
- DDR4 devices
- Motherboards capable of using DDR4
- DIMMs and LRDIMMs
- DDR controllers capable of DDR4 protocol and speed
- PHYs capable of DDR4 speeds and PHY standard
- POD12 I/Os Enabled by TSMC OIP and Cadence
- Design kits for DDR4 packages and PCBs
- Update to DFI standard (controller-PHY interface)
- Memory Models Enabled by Cadence

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Memory Controller Evolution



- Many clients in the system that previously had their own dedicated memory now share a single external memory
- Driving force: high-speed, low-cost memory
 - 2 billion transistor DRAM chips as low as \$1

8

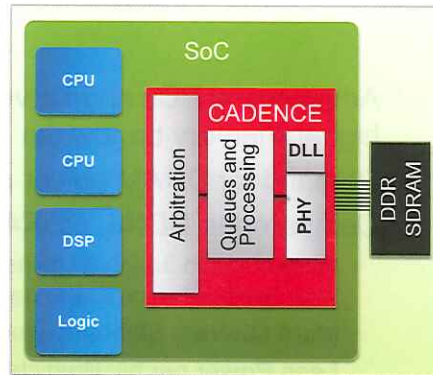
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What Makes a Good Memory Controller?

*Improving system performance,
reducing cost, reducing power*

1. TTI: Allow multiple clients to share a single memory
2. Performance: Low latency for critical transactions
3. Performance: High bandwidth for large transfers
4. Performance: Reorder transactions for approximately 30 percent bandwidth gain
5. Power: Use low-power modes and access methods to control DRAM power
6. Features: Broad and deep feature set meets market needs



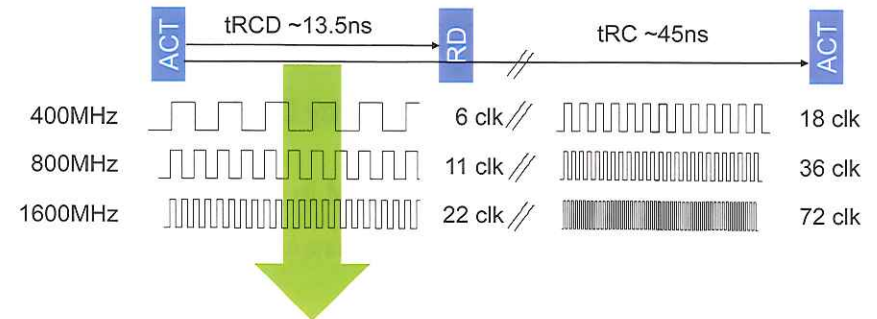
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High-Speed DDR3 and DDR4 Challenges

- DDR latency is longer than ever
 - Staying constant in ns, but increasing by clock cycles
- DDR controller intelligence now more critical than ever



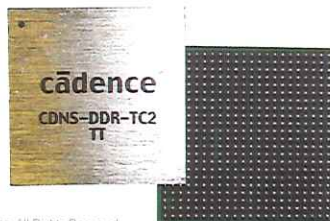
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TSMC 28HPM and 28HP DDR Test Chips

- TSMC-Cadence collaboration will produce first silicon-proven DDR4 IP in TSMC28nm
- TSMC28HP silicon worked on test board in August
- Fully functional High Speed PHY and Controller
 - Working in silicon on both 28HP and 28HPM test chips
 - Supporting DDR4, DDR3, DDR3L



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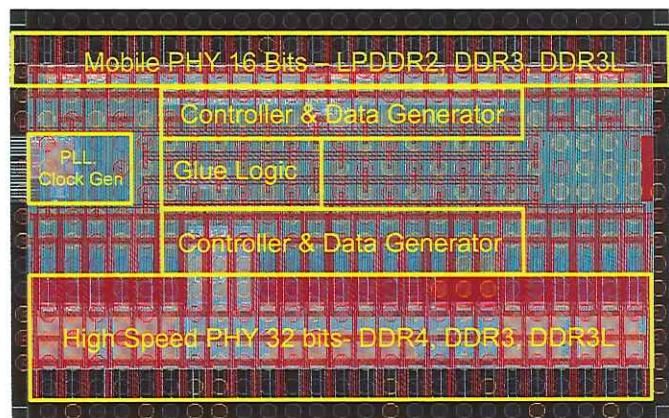
TSMC 28HPM and 28HP DDR Test Chips

- HPM silicon back first week of July 2012
- Full functional Mobile PHY and controller
 - Supporting DDR3, LPDDR2 and DDR3L
 - DDR-1600 speed achieved by our all-digital DLL PHY
 - Low area – just 0.029mm² per 8-bit data slice (not including IO)
 - Low power
 - Power further reduced by introduction of multiple power modes
 - Fully functional DDR IOs
 - Mature characterization environment and software
 - Took only 3 days to achieve stable operation from first power-on
- TSMC 20SoC PHYs in planning stage

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TSMC 28HPM Test Chip Modules



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Low Power Memory: LPDDR3 Adds Bandwidth Over Existing LPDDR2 Technology

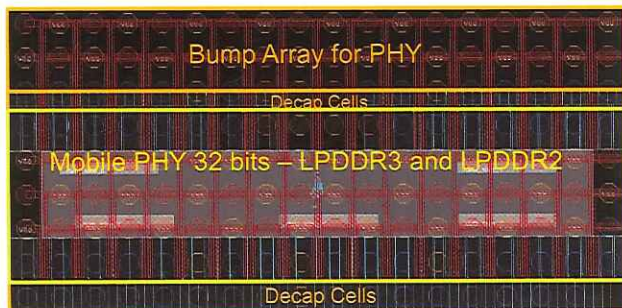
LPDDR2	LPDDR3
Specification release 2009	Specification release May 2012
DDR-1066 (533MHz)	DDR-1600 (800MHz) – 50% increase
1.2v HSUL Unterminated I/Os	1.2v HSUL I/O with On-Die Termination (ODT)
Read training	Read training, Command/Address (CA) training and Write Leveling
I/O Capacitance 2.5pF	I/O Capacitance 1.8pF
Low Power consumption	Expected to be less from lower I/O capacitance and more advanced process

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28HPM DLL PHY 32 Bits Supporting LPDDR2/LPDDR3



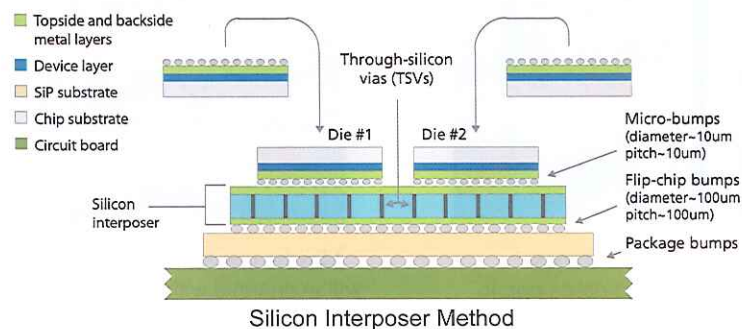
Taped out August 2012 with LPDDR3 and LPDDR2 support

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What is Wide-IO DRAM?

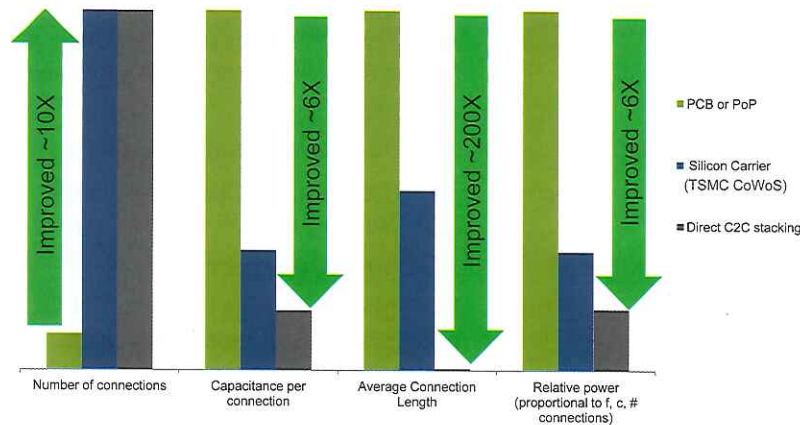
- DRAM prepared for die-to-die connection using TSV
 - Connected to CPU using Silicon Interposer or direct chip-to-chip stack



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TSV Benefits



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LPDDR3 Vs. Wide-I/O - Characteristics

Attribute	LPDDR3	Wide I/O
Bandwidth per die	51.2Gbit/s (X32)	102.4Gbit/s
Bandwidth per package	102.4Gbit/s (dual-channel)	102.4Gbit/s
Dies per package	Up to 4 (in theory)	Up to 4 (in theory)
System configurations	PoP or normal PCB interconnect	Silicon Interposer or direct chip-to-chip
General	Improved, Evolutionary Technology	New, Revolutionary Technology
Compatibility	Backwards compatible with LPDDR2	May be forwards compatible with Wide-IO2

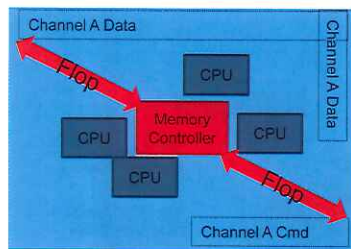
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SoC Construction

LPDDR3:

- PoP Ballout dictates SoC Construction
- Command and data separated 5-15mm on the SoC?

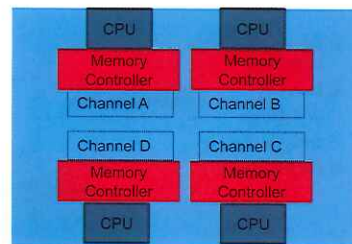


Note: Only one channel shown

- Extra pipeline flop stages required to transmit data edge to edge; adds latency and power

Wide I/O:

- TSV Ballout dictates SoC Construction
- Each channel contained within 2.5mm



- May be possible to reach all IOs within channel without pipelining

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System Power Comparison

Attribute	LPDDR3 2Channel	Wide I/O
Peak Bandwidth	102Gbit/s	102Gbit/s
Core power	Predicted to be similar for both technologies	
I/O Voltage	1.2V	1.2V
I/O Capacitance	1.8pF	0.5pF
Full-bandwidth, all chip I/O Power ($1/2 f c v^2$)	$64 \cdot 0.5 \cdot 1600 \cdot cv^2 = 51200cv^2$	$512 \cdot 0.5 \cdot 200 \cdot cv^2 = 51200cv^2$
First-order approximation:	the difference in IO power is proportional to c	
Powerdown, Self-Refresh and DPD capability	One power state for each channel, one channel per die, 1-2 channels per system	4 channels per die
SoC Power	PHY may require DLL/PLL	DLL/PLL not required

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Wide-I/O Maturity and Ecosystem

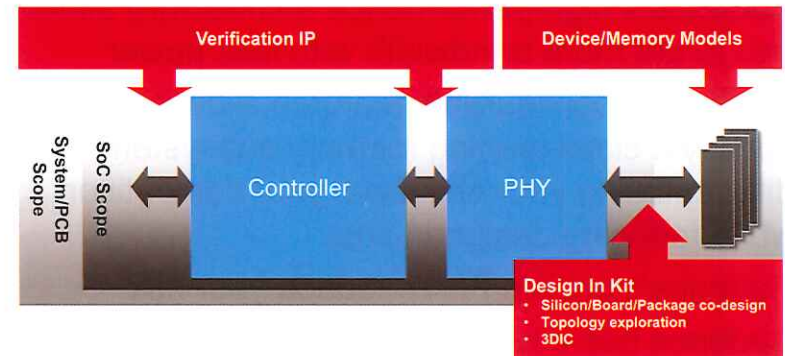
- TSMC showed CoWoS chips at 2012 DAC
- Cadence Wide-I/O DRAM Controller
 - Includes expanded MBIST tests for Wide-I/O
 - Deployed on two projects
 - First IP to market in November 2010
- Cadence Wide-I/O PHY
 - Deployed on one project – first delivery August 2011
- Cadence Wide-I/O Memory Models (Verification IP)
- TSMC Reference Flow 12 Supports Cadence 3D IC

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Integration is a Major Customer Challenge

Cadence delivers fully integrated solutions spanning IP, services, and tools

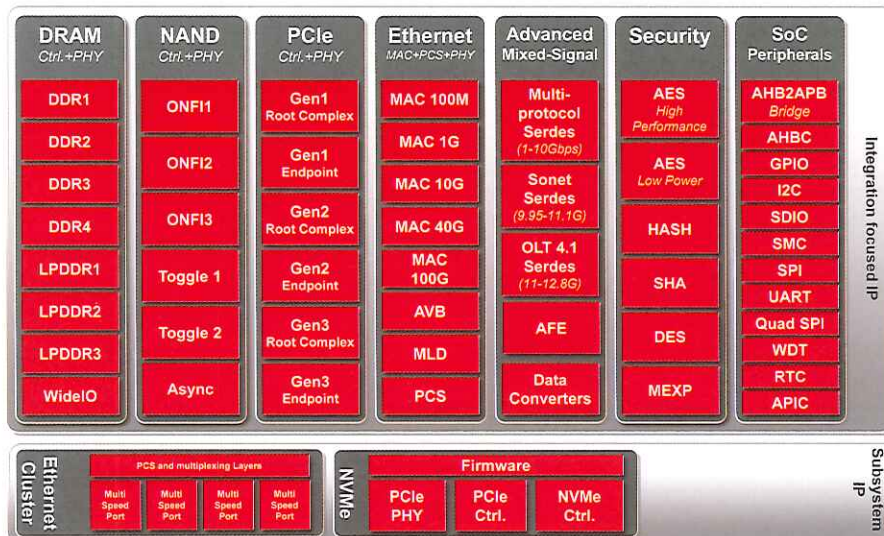


- IP integration is a significant effort for customers, and a source of many design problems
- Well integrated controllers and PHY's are critical, but not sufficient
- Verification IP and memory models ensure system works correctly first time for time-to-market sensitive applications
- Links to silicon/package/board become critical with high-speed interfaces

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Cadence Rapidly Expanding IP Portfolio



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Cadence Design IP Success

DDR	<ul style="list-style-type: none"> • First with DDR4 and LPDDR3 • 100+ DDR3 design wins • 400+ total DDR design wins • 3100+ configurations delivered
WideIO	<ul style="list-style-type: none"> • First to be silicon proven with full 3D packaging
Flash	<ul style="list-style-type: none"> • First with ONFI3/Toggle2 • 50+ design wins • >95% theoretical device throughput
PCIe	<ul style="list-style-type: none"> • 25+ design wins • Silicon proven X8 and X16 Gen3
Ethernet	<ul style="list-style-type: none"> • 50+ customers • UNH certified
Advanced Mixed-signal	<ul style="list-style-type: none"> • 200+ tapeouts • 65+ SerDes designs • 200+ data converters • 70+ nodes and process variations

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Conclusion

- Cadence's high-performance architecture allows you to get more bandwidth with less power
- Cadence's configurable features allow you to specify a class-leading memory subsystem, differentiating your chip from your competition, while reducing design-in time
- Cadence's proven PHYs reduce your risk
- Cadence has a high-quality memory controller and PHY with more than 400 design wins – we are the experts!

A large version of the Cadence logo, featuring the word "cadence" in a lowercase, sans-serif font. A small red horizontal bar is positioned above the letter "a".

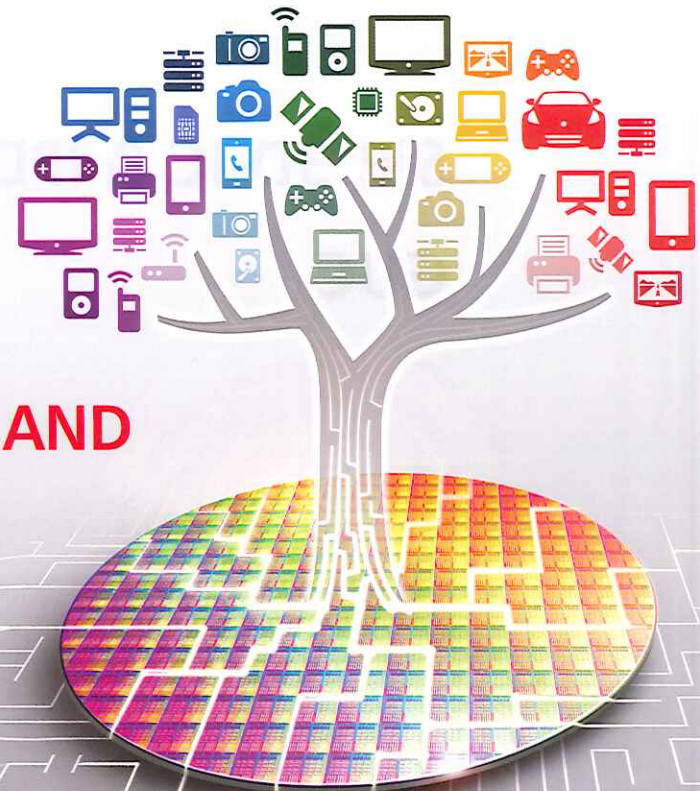
NOTE

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This image shows a single sheet of white paper with horizontal ruling lines. The lines are evenly spaced and run across the width of the page. There are no margins, text, or other markings on the paper.

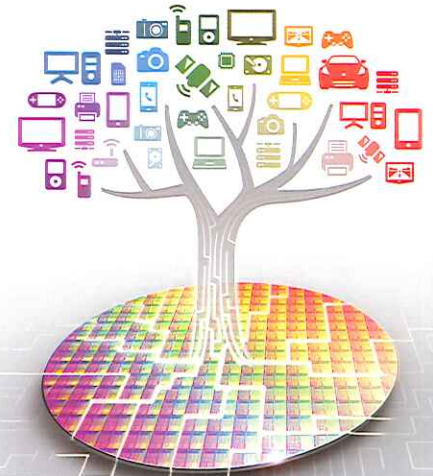
EDA / IP / Services Track

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CAPACITY PROVIDER**



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SiP, 3D-IC & IPD Complement Flexible ASICs GUC



ABSTRACT

The integration in a chip of non-logic functions, such as memory, analog, RF, MEMS and BIO, is becoming more difficult and cost inefficient as CMOS technology advances into deep submicrons nodes.

System-in-Package (SiP), in side by side and/or stack configurations, enables heterogeneous integration and complements the Flexible ASIC model. GUC has been developing SiP since 2004 and has become an acknowledged technology leader with SiP accounting for around 30% of the company's Turnkey revenue over the past 3 years.

Today's 3D-ICs using through Silicon Vias (TSVs) are emerging as proven, viable technologies, offering compelling advantages in power, performance, miniaturization, and time-to-market, as well as easing the continuation of Moore's Law beyond the 14nm node. With chip/package/board design & simulation expertise and known good die (KGD), thermal and mechanical solutions, and process fine tuning capabilities, GUC has established CoWoS capabilities by working with TSMC and is planning to launch its CoWoS design service as soon as TSMC starts offering CoWoS service.

The booming Mobile Internet Devices (MID) applications are triggering package form factor and thickness miniaturization. SiP, 3D-ICs are the best approaches to fulfill the market's requirement. In addition to the service for active devices, GUC also provides the service of Integrated Passive Device (IPD) with silicon substrate to integrate and miniaturize the same miniaturization requirement for passive devices, especially those for RF products of MID applications. GUC has started offering IPD service since Q1'12.





SiP, 3D IC & IPD Complement Flexible ASICs

Charles Lin, Advanced Package Planning

Outline

- GUC & The Flexible ASIC Business Model
- SiP Differentiates Flexible ASIC Service
- GUC's Unique SiP Value
- Integrated Passive Device (IPD), Chip-on-Wafer-on-Substrate (CoWoS™) and 3D IC Results
- Summary

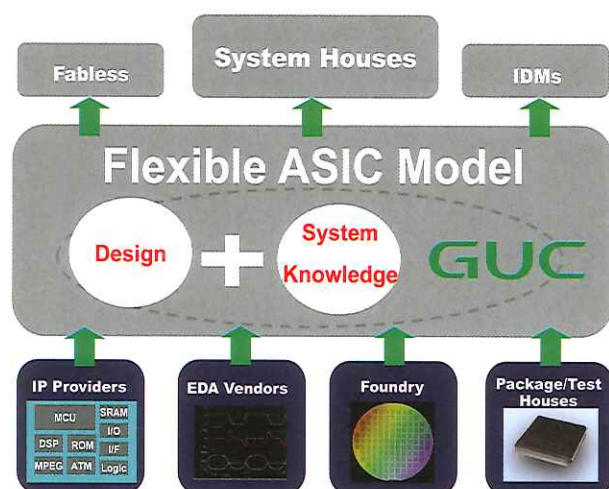
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The Flexible ASIC Model



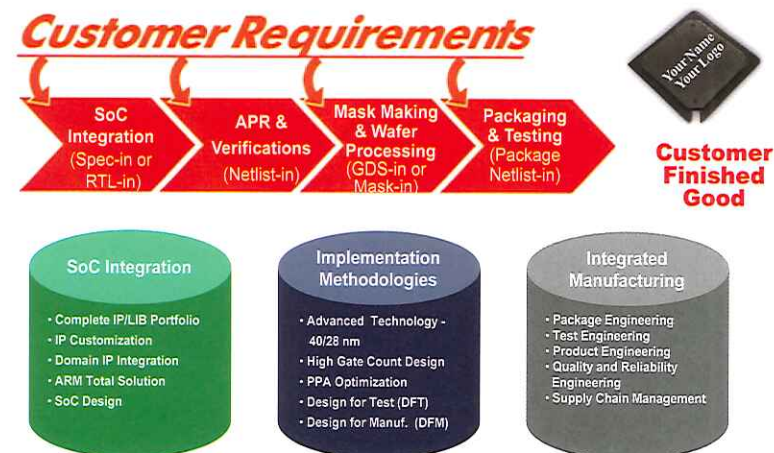
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GUC's Flexible ASIC Services



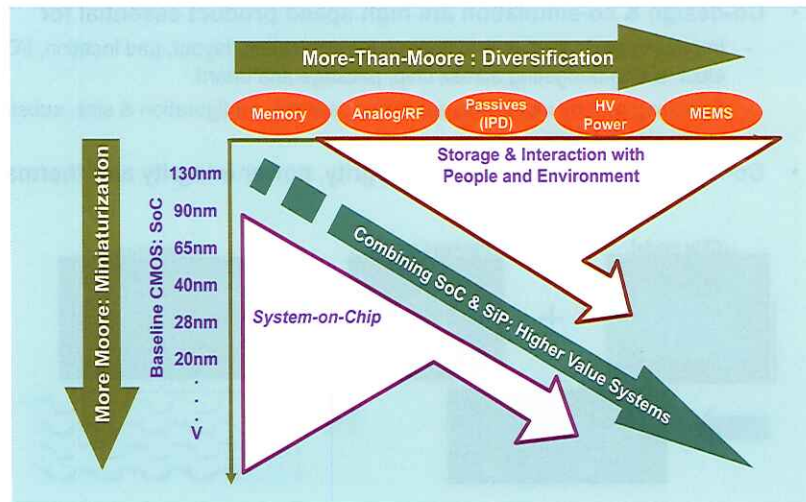
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SiP Complements SoC



P5

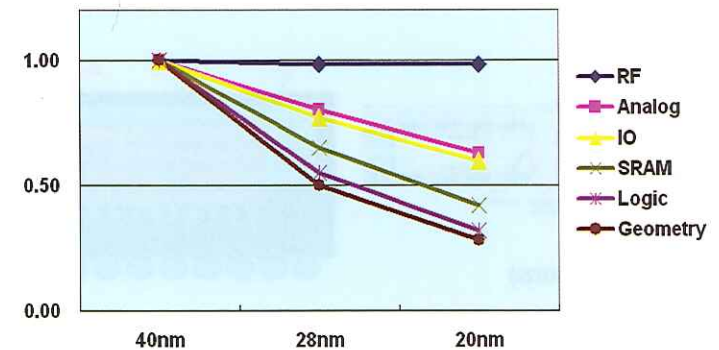
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Non-CMOS Scaling Effectiveness Is Decreasing

- Non-CMOS scaling is becoming more difficult and less effective as CMOS technology beyond 28nm
- Performance degrades



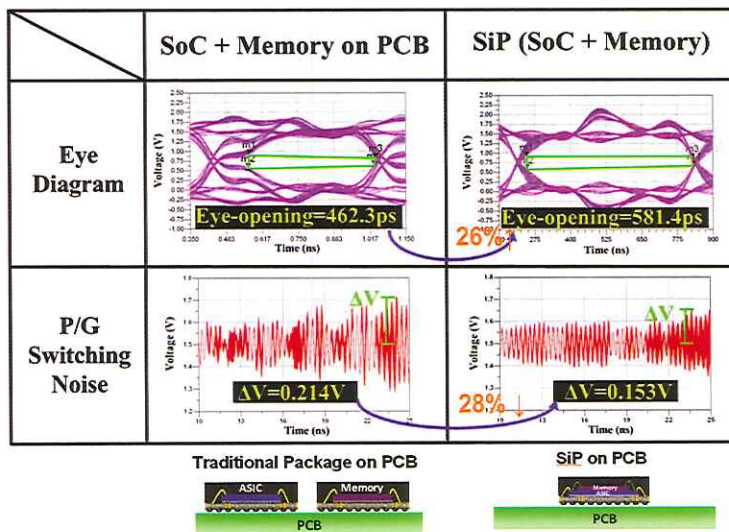
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SiP Enhances Product Competitiveness



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3D SiP Challenges

- Known Good Die(KGD) Availability and Logistics
 - Chip/Package/Board co-design & co-simulation
 - Thermal Solution
 - Total Test Solution
 - Failure Analysis Capability
- GUC provides effective solutions for all of these
 - 3D SiP experience and capability is invaluable for implementing CoWoS, and 3D IC Through Silicon Via (TSV) technology

P8

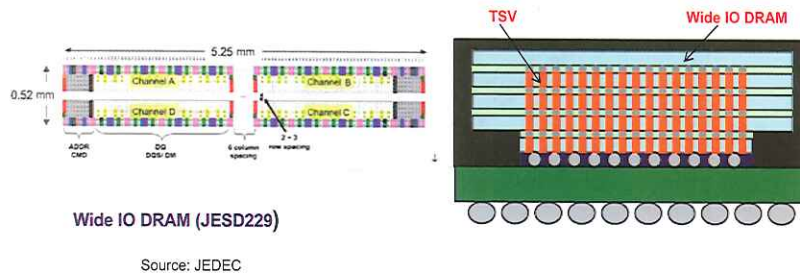
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Availability and Logistics of KGD

- KGD availability is the prerequisite of SiP implementation
- Non-CMOS KGDSs are even more difficult
- Robust KGD logistics capability is required for SiP success
- Wide IO DRAM is believed to be the best memory KGD solution in TSV era



P9

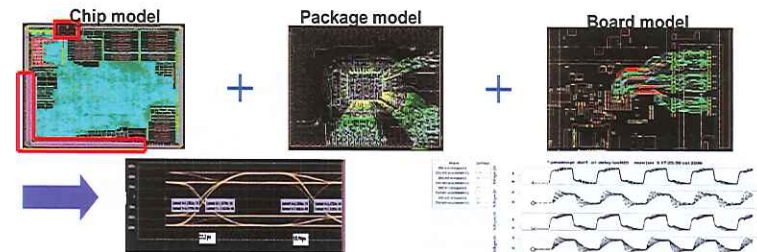
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Chip-Package-Board Co-Design/Simulation

- **Co-design & co-simulation are high speed product essential for**
 - Improving performance thru floor plan optimization, layout, pad location, I/O and elect. timing budgeting across chip, package and board
 - Reducing cost by identifying optimized package configuration & size, substrate, board size & layers
- **Co-simulation includes signal integrity, power integrity and thermal**



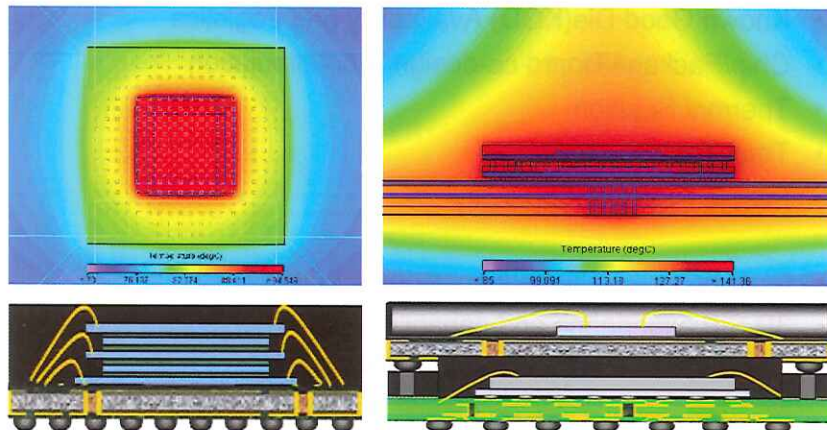
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3D Thermal Simulation



Thermal solution is more critical for SiP/3DIC than for single chip package

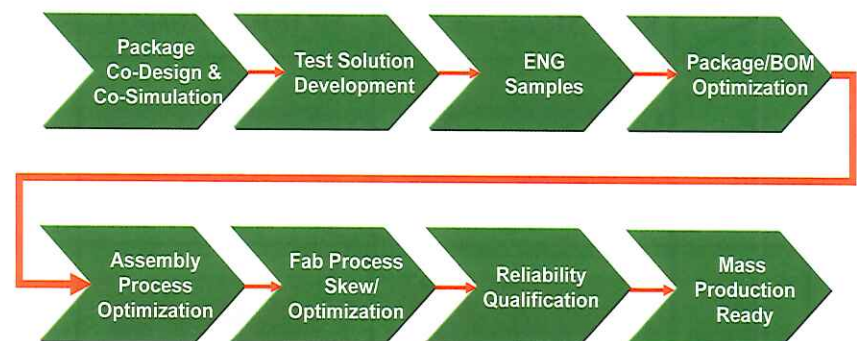
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A Complicated and Lengthy Journey From Package Design to Mass Production



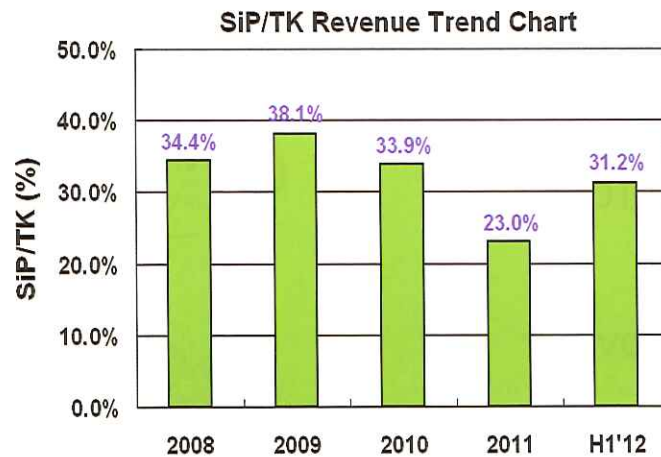
SiP/3D IC are even more difficult. GUC has gained valuable experience through proven product implementations

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SiP Contributes Significant TK Revenue



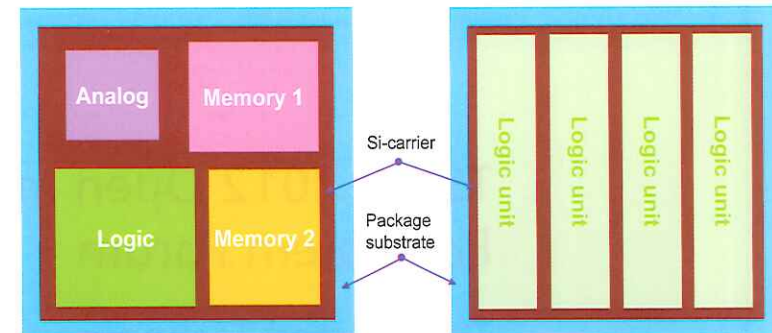
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CoWoS Service & Potential Applications



GUC plans to offer CoWoS service soon after process release

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Summary

- GUC, The Flexible ASIC Leader™, has developed SiP as a differentiator to enhance product competitiveness
- Has offered IPD service since Q1'12
- GUC will transition SiP design and production experience into advancing to CoWoS, and 3D IC TSV services

P15

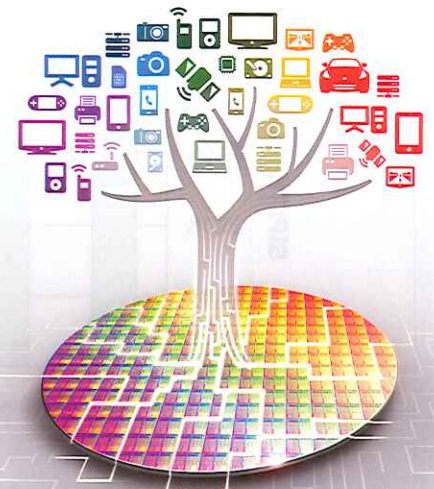
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Timing Sign-off and Technology Migration Using Functionalized Timing Reports

IMEC



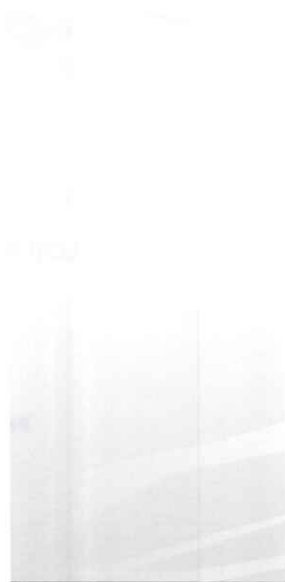
ABSTRACT


The increasing complexity of advanced technology nodes has resulted in an intimidating range of options available to designers (threshold voltage, supply voltage, gate length bias, library track height, etc.) and also in an increase in the number of “recommended” process corners (worst case, worst case low temperature, best case, max leakage, etc.) required for timing sign-off within each option. TSMC and imec, through its Technology Targeting Service, are collaborating to help customers make informed decisions about the many option choices at the early stages of design and also to quickly flag potentially problematic process corners at the later stages of design.

One of the results of this collaboration is functionalized timing reports, referred to as traces. Traces capture the structure of critical data paths within a design but differ from traditional static timing reports in that they take the standard cell libraries (Liberty files) associated with different process corners as input arguments. Traces re-calculate library-dependent information, such as interconnect loads and cell delays, using internal functions to access the library data to produce critical path delays for different process corners with processing times measured in seconds and accuracies of approximately 1%, when compared with standard synthesis/STA flows. The goal is not to replace standard timing analysis methods, but rather to quickly assess all available TSMC process corners for a given option and to flag previously unsuspected process corners as potentially problematic and in need of further attention, in addition to the recommended corners.

The concept of dynamic traces has also been applied to the timing analysis of designs implemented in different technology nodes. Examples will be given of traces generated from a design during synthesis using a reference technology, option and corner (for example, 40nm LP worst-case) and functionalized to permit timing analysis for both older (65nm LP and 90nm GP) and more advanced (28nm HP) technologies with approximately 5% accuracy, when compared to standard synthesis/STA flows. An important advantage of trace construction is that it only requires access to an existing reference timing report and not to the design IP itself. In addition, the processing time required for trace analysis is largely independent of the size of the design and only on the logic depth of the data-paths.


The use of these techniques further enhances TSMC and imec’s ability to work with partners to target the right technology for their design (providing up-front performance evaluation of different process nodes and options within days) and to avoid missed tape-out deadlines (rapid assessment of all corners, rather than only the recommended corners).





Timing Sign-off and Technology Migration using Functionalized Timing Reports

Phillip Christie



OVERVIEW

IMEC's technology profile

TSMC & IMEC TRACE analysis collaboration

- What is the problem?
- What is a TRACE?
- Use cases

Summary

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2

IMEC

IMEC ENERGY	IMEC HUMAN++	IMEC GREEN RADIO	IMEC NVISION
IMEC SYSTEMS FOR INDUSTRIAL APPLICATIONS	IMEC CORE CMOS	IMEC CMORE	IMEC SERVICES

- Founded 1984
- Independent
- Providing in
- Global part

Design Services	<ul style="list-style-type: none"> ✓ Front & Back End Digital design ✓ Mixed signal design ✓ Custom standard cell libraries
ASIC Services	<ul style="list-style-type: none"> ✓ TSMC value chain aggregator ✓ Dedicated foundry account managers ✓ Foundry data-bases (0.5um – 28nm) on local servers ✓ Packaging, test, qualification
EDA Flows	<ul style="list-style-type: none"> ✓ Cadence ✓ Synopsys ✓ Mentor



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TSMC AND IMEC SERVICES COLLABORATE ON TRACE ANALYSIS

- Increasing number of TSMC recommended signoff corners for designs
- Increasingly tight deadlines can lead to critical corners for a specific design being missed

TSMC Europe Field Technical Support collaboration with IMEC to develop rapid techniques for flagging potentially problematic corners

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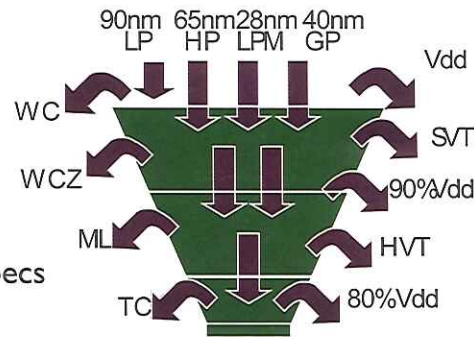
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WHAT IS THE PROBLEM?

Rapid assessment of

- Technology nodes
- Node options
- Variability

to meet your performance specs



At an early enough phase in the design flow to be useful!

TAPE OUT DEADLINES AS USUAL?

- Are TSMC performance tables accurate enough for your design, WC sign-off selections, performance estimates ?
- Can your gurus master the large range of technology options of the advanced 65, 40 & 28nm nodes?
- Or do you try out all the different technology options by expensive and time consuming simulations ?

Performance/power/area benchmark
G/LP Technologies

	90nm	65nm	40nm	28nm	16nm	10nm
V _{DD}	1.0	0.9	0.8	0.7	0.6	0.5
V _{DD} (min)	0.9	0.8	0.7	0.6	0.5	0.4
Gate density	1000	2000	4000	8000	16000	32000
Speed	1000	2000	4000	8000	16000	32000
Power	1000	2000	4000	8000	16000	32000
Power (W)	1000	2000	4000	8000	16000	32000
Leakage	1000	2000	4000	8000	16000	32000
Power (W)	1000	2000	4000	8000	16000	32000



EDA tool flows are designed to optimize the design for a fixed technology

They are not designed to optimize the technology for a fixed design



WHAT IS A TRACE?

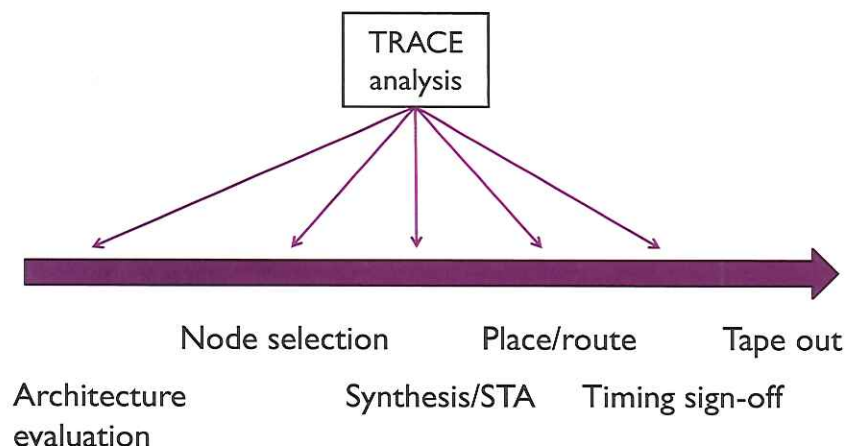
TRACE generation

- Use a timing report from one standard PVT timing simulation produced by standard CAD tools (HOURS)
- Generate "TRACE": an active timing report which takes PVT corners as inputs
- Run the TRACE in other PVT corners (SECONDS)

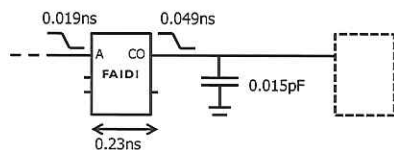
What are the benefits ?

- Analyses of each corner performed in seconds
- Trace analysis time independent of the size of the design
- Do not require access to design IP

TRACE APPLICATIONS



A STANDARD TIMING REPORT IS USED TO GENERATE A TRACE



Cell	inPin (r/f)	inTrans	outPin (r/f)	outTrans	FanOut	Cap	Delay
FA1D1	A (f)	0.019	CO (f)	0.049	1	0.015	0.23

A timing report is a passive text file generated for a fixed technology

HOW DOES IT WORK? TIMING TRACE GENERATION

Report segment

Cell	inPin (r/f)	inTrans	outPin (r/f)	outTrans	FanOut	Cap	Delay
FA1D1	A (f)	0.019	CO (f)	0.049	1	0.015	0.23



Trace segment

```
[delay(5) , tran(5) ] = timing(lib, 'FA1D1', 'A', 'f', 'CO', 'f', cap, tran(4))
```

A Timing TRACE is an active timing report using library (liberty) files as inputs

TRACES ARE SIMPLE TO USE

```
>> eightbitx --lib tcbn40lpbwpwc.lib
```

```
>> ls
tcbn40|pbwpc0d99.lib      tcbn40|pbwplvtm.lib      tcbn40|pbwpmgl.lib
tcbn40|pbwpccli.lib       tcbn40|pbwplvtc0d9.lib   tcbn40|pbwpmli.lib
tcbn40|pbwplvt0d99.lib   tcbn40|pbwplvtcli.lib   tcbn40|pbwptc0d9.lib
tcbn40|pbwplcli.lib       tcbn40|pbwplvtwc0d81.lib tcbn40|pbwptcli.lib
tcbn40|pbwplvtbc0d99.lib tcbn40|pbwplvtwc0d81.lib tcbn40|pbwptwc0d81.lib
tcbn40|pbwplvtbcli.lib   tcbn40|pbwplvtwccli.lib tcbn40|pbwptwc0d81.lib
tcbn40|pbwplvttd099.lib  tcbn40|pbwplvtwc0d81.lib tcbn40|pbwptwcli.lib
tcbn40|pbwplvttdcli.lib  tcbn40|pbwplvtwc0d81.lib tcbn40|pbwptwcli.lib
tcbn40|pbwplvtm0d99.lib  tcbn40|pbwplvtwccli.lib tcbn40|pbwptwc0d81.lib
tcbn40|pbwplvtmcli.lib   tcbn40|pbwplvtwc0d99.lib tcbn40|pbwptwcli.lib
```

```
>> eightbitx --lib tcbn40lpbwpwc.lib
```

Critical path delay = 1.4031, path 1

```
>> eightbitx --lib tcbn40lpbwpwcz0d81.lib
```

Critical path delay = 4.6497, path 1

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Standard Unix command-line interface

TRACES ARE SIMPLE TO USE

```
>> eightbitx --lib tcbn40lpbwpwcz0d81.lib --verbose
```

```
>> eightbitx --lib tcbn40lpbwwwpcz0dS1.lib --verbose
```

```

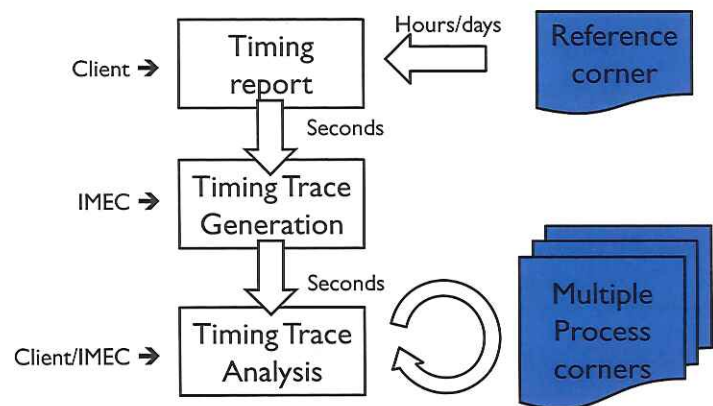
DFQD04: ip 'C', inrf 'r', op 'Q', outCnt = 0.0038996, itran 0, atan 0.11164 when "N/A", delay 0.58469, when "N/A", 1 arc(s)
CND04: ip 'C', inrf 'r', op 'ZIN' outfr 'f', cloud 0.0047244, itran 0.11164, atan 0.097252 when "N/A", delay 0.11696, when "N/A", 1 arc(s)
NRK2D3: ip 'A1', inrf 'r', op 'ZIN' outfr 'f', cloud 0.0013033, itran 0.097252, atan 0.052719 when "N/A", delay 0.083853, when "N/A", 1 arc(s)
FA1D1: ip 'A1', inrf 'r', op 'CO' outfr 'f', cloud 0.0010033, itran 0.052719, atan 0.12366 when "B8C1", delay 0.73951, when "B8C1", 2 arc(s)
FA1D1: ip 'A1', inrf 'r', op 'CO' outfr 'f', cloud 0.0016656, itran 0.12366, atan 0.13365 when "B8C1", delay 0.7975, when "B8C1", 2 arc(s)
FA1D1: ip 'A1', inrf 'r', op 'CO' outfr 'f', cloud 0.0049429, itran 0.0049429, atan 0.1655 when "B8C1", delay 0.84896, when "B8C1", 2 arc(s)
NRK2D4: ip 'A1', inrf 'r', op 'ZIN' outfr 'f', cloud 0.0043471, itran 0.1655, atan 0.14412 when "N/A", delay 0.1738, when "N/A", 1 arc(s)
IMVD4: ip 'A1', inrf 'r', op 'ZIN' outfr 'f', cloud 0.0031038, itran 0.14412, atan 0.060544 when "N/A", delay 0.10874, when "N/A", 1 arc(s)
ND2D4: ip 'A1', inrf 'r', op 'ZIN' outfr 'f', cloud 0.0019677, itran 0.060544, atan 0.066665 when "N/A", delay 0.076342, when "N/A", 1 arc(s)
CND2D4: ip 'A1', inrf 'r', op 'ZIN' outfr 'f', cloud 0.0018195, itran 0.066665, atan 0.082762 when "N/A", delay 0.093525, when "N/A", 1 arc(s)
FA1D1: ip 'A1', inrf 'r', op 'CO' outfr 'f', cloud 0.0009712, itran 0.082762, atan 0.2089 when "A1A2", delay 0.21, when "A1A2", 1 arc(s)
OAI21D1: ip 'B', inrf 'r', op 'ZIN' outfr 'f', cloud 0.0013825, itran 0.2089, atan 0.18842 when "A1A2", delay 0.27053, when "A1A2", 3 arc(s)
CQKOR2D2: ip 'A1', inrf 'r', op 'Z' outfr 'r', cloud 0.000856, itran 0.18842, atan 0.088827 when "A2", delay 0.38149, when "A2", 2 arc(s)
DFQD02: ip 'C', op 'D', inCnt 0, outCnt 0.088827, rtfup, setup 0.19236
arrivalTime(1) = 4.4574
setUpTime = 0.19236
outTime(1) = 4.6589

```

Critical path delay = 4.6497, path 1

--verbose output option for report re-generation

TIMING SIGN-OFF ANALYSIS



Problematic corners flagged quickly

SETUP TIME BENCHMARKING

100 paths, Reference library 40lpwc, averageTRACE error 1.4%

Library	Wireload	Vdd (V)	Temp (C)	Delay Trace (ns)	Delay STA (ns)	Error
40lplt	Agr	1.21	-40	0.9337	0.9242	1.0%
40lpgc	Agr	1.21	0	0.9519	0.9390	1.4%
40lplt	Con	1.21	-40	0.9445	0.9434	0.1%
40lpgc	Con	1.21	0	0.9642	0.9588	0.6%
40lpml	Agr	1.21	125	0.9990	0.9756	2.4%
40lpml	Con	1.21	125	1.0168	1.0091	0.8%
40lpmig	Agr	1.21	125	1.0487	1.0352	1.3%
40lpmig	Con	1.21	125	1.0653	1.0560	0.8%
40lpml0d99	Agr	0.99	125	1.4559	1.4327	1.6%
40lpit0d99	Agr	0.99	-40	1.4611	1.4409	1.4%
40lpgc0d99	Agr	0.99	0	1.4617	1.4556	0.4%
40lpit0d99	Con	0.99	-40	1.4759	1.5106	-2.3%
40lpml0d99	Con	0.99	125	1.4783	1.5106	-2.1%
40lpgc0d99	Con	0.99	0	1.4759	1.4903	-1.0%
40lptc	Agr	1.1	25	1.5336	1.5244	0.6%
40lptc	Con	1.1	25	1.5481	1.5649	-1.1%
40lpwc	Agr	0.99	125	2.7125	2.7473	-1.3%
40lpwc	Con	0.99	125	2.7245	2.7624	-1.4%
40lptc0d9	Agr	0.9	25	2.8709	2.8409	-1.1%
40lptc0d9	Con	0.9	25	2.9084	2.9674	-2.0%
40lpwc	Agr	0.99	0	3.0764	3.0581	0.6%
40lpwc	Con	0.99	0	3.098	3.1447	-1.5%
40lpwcl	Agr	0.99	-40	3.2516	3.2051	1.5%
40lpwcl	Con	0.99	-40	3.2751	3.3445	-2.1%
40lpwc0d81	Agr	0.81	125	5.7233	5.6818	0.7%
40lpwc0d81	Con	0.81	125	5.7394	5.988	-4.1%
40lpwc0d81	Agr	0.81	0	9.0226	9.1743	-1.7%
40lpwc0d81	Con	0.81	0	9.2566	9.5238	-2.8%

DESIGN-DEPENDENT SET-UP TIME ORDERING

8bit multiplier

DSP (512K gates)

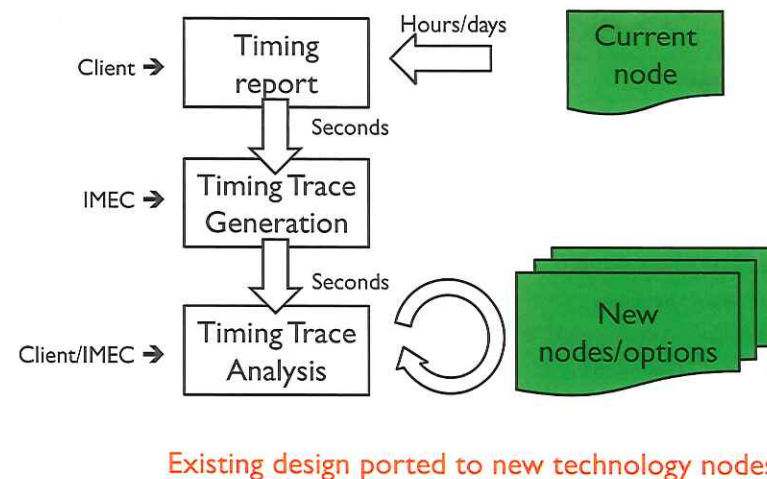
Corner name	Delay (ns)	Voltage (V)	Temp (C)	Corner name	Delay (ns)	Voltage (V)	Temp (C)
tcbn40lpbwpwcl_con	1.71	0.99	-40	tcbn40lpbwpwcl_con	4.66	0.99	-40
tcbn40lpbwpwcl_agr	1.68	0.99	-40	tcbn40lpbwpwcl_con	4.38	0.99	-40
tcbn40lpbwpwcl_con	1.62	0.99	125	tcbn40lpbwpwcl_agr	4.07	0.90	125
tcbn40lpbwpwcl_agr	1.59	0.99	125	tcbn40lpbwpwcl_con	3.80	0.99	125
tcbn40lpbwpwcl0d99_con	1.52	0.90	125	tcbn40lpbwpwcl_agr	3.25	0.99	125
tcbn40lpbwpwcl0d99_agr	1.48	0.90	125	tcbn40lpbwpwcl_con	3.08	0.99	125
tcbn40lpbwpwcl0d99_con	1.43	0.99	125	tcbn40lpbwpwcl_agr	2.87	0.90	125
tcbn40lpbwpwcl0d99_agr	1.40	0.99	125	tcbn40lpbwpwcl_con	2.71	0.99	125
tcbn40lpbwpwcl0d99_con	0.80	1.10	25	tcbn40lpbwpwcl_agr	2.15	1.10	25
tcbn40lpbwpwcl0d99_agr	0.79	1.10	25	tcbn40lpbwpwcl_con	2.05	0.99	25
tcbn40lpbwpwcl0d99_con	0.77	0.99	25	tcbn40lpbwpwcl_agr	2.04	0.99	25
tcbn40lpbwpwcl0d99_agr	0.77	0.99	25	tcbn40lpbwpwcl_con	2.02	0.99	25
tcbn40lpbwpwcl0d99_con	0.76	0.99	125	tcbn40lpbwpwcl_agr	1.53	1.10	125
tcbn40lpbwpwcl0d99_agr	0.75	0.99	125	tcbn40lpbwpwcl_con	1.46	0.99	125
tcbn40lpbwpwcl0d99_con	0.75	0.99	125	tcbn40lpbwpwcl_agr	1.46	0.99	125
tcbn40lpbwpwcl0d99_agr	0.75	0.99	125	tcbn40lpbwpwcl_con	1.46	0.99	125
tcbn40lpbwpwcl0d99_con	0.54	1.21	-40	tcbn40lpbwpwcl_agr	1.45	1.21	-40
tcbn40lpbwpwcl0d99_agr	0.54	1.21	-40	tcbn40lpbwpwcl_con	1.38	1.21	-40
tcbn40lpbwpwcl0d99_con	0.52	1.21	-40	tcbn40lpbwpwcl_agr	1.31	1.21	-40
tcbn40lpbwpwcl0d99_agr	0.51	1.21	-40	tcbn40lpbwpwcl_con	1.29	1.21	-40
tcbn40lpbwpwcl0d99_con	0.49	1.21	0	tcbn40lpbwpwcl_agr	1.05	1.21	0
tcbn40lpbwpwcl0d99_agr	0.49	1.21	0	tcbn40lpbwpwcl_con	1.00	1.21	0
tcbn40lpbwpwcl0d99_con	0.48	1.21	0	tcbn40lpbwpwcl_agr	0.95	1.21	0
tcbn40lpbwpwcl0d99_agr	0.48	1.21	0	tcbn40lpbwpwcl_con	0.93	1.21	0

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NODE/OPTION MIGRATION



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NODE SELECTION

8bit-multiplier, aggressive wire-loads, 100 paths

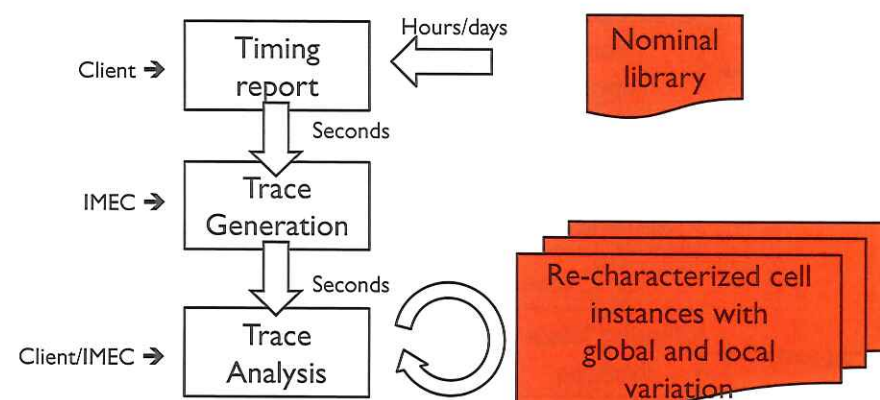
Reference Library	Target Library	Design Compiler (ns)	Timing Trace (ns)	Error
tcbn40lpbwpwcl	tcbn40lpbwpwcl	1.326	1.336	0.7%
tcbn40lpbwpwcl	tcbn40lpbwpwcl	0.758	0.752	0.8%
tcbn40lpbwpwcl	tcbn40lpbwpwcl	0.463	0.481	3.8%
tcbn40lpbwpwcl	tcbn40lpbwpwcl	7.576	7.248	-4.3%
tcbn40lpbwpwcl	tcbn40lpbwpwcl	0.389	0.399	2.6%
tcbn40lpbwpwcl	tcbn28hpwpwcl	0.677	0.671	0.9%
tcbn40lpbwpwcl	tcbn65lpwcl	1.515	1.435	-5.2%

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VARIABILITY ANALYSIS



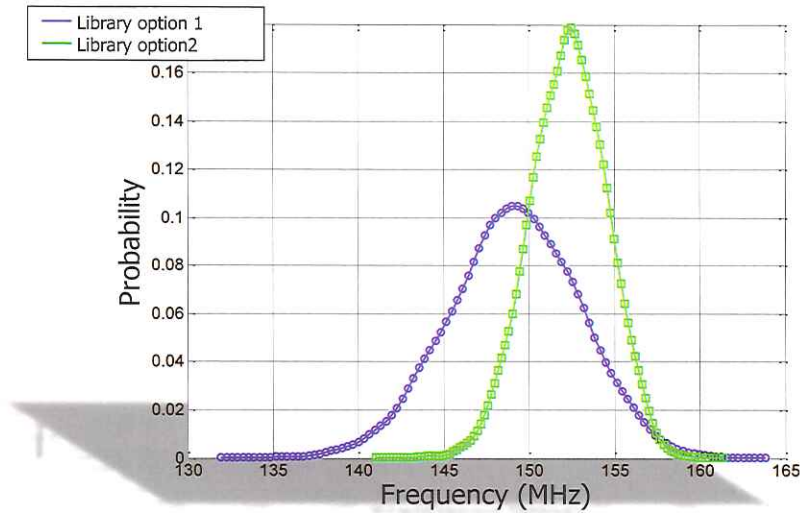
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TIMING VARIABILITY USING TRACES

DSP54 40nm LP SVT, Typical Case



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SUMMARY

- TRACES can flag a design's potentially troublesome process corners for more detailed analysis
- TRACES are generated from client's timing report using trace generation tool
- TRACE run time is sub-second and independent of the size of the design
- ~1% timing accuracy

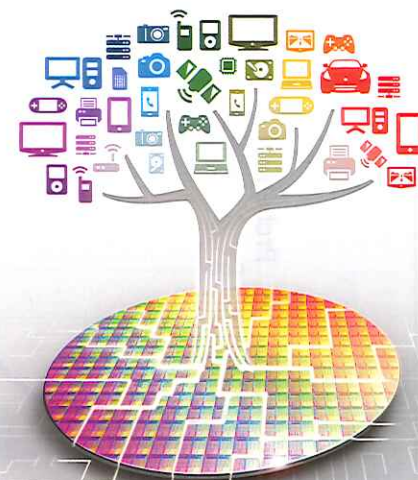
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The Trusted Technology and Capacity Provider



Truly Differentiated Memory Subsystems on TSMC's Advanced Technology Nodes eSilicon

ABSTRACT

As the three C's—convergence of computers, communication and content (multimedia) continue, they increase memory content in SoCs. SoCs aggregate functionality with multiple CPUs, which must run at stringent power and performance specifications. This increased functionality is also driving a constant increase in memory content in every chip design.

TSMC's advanced process technologies are enabling a high level of functionality in today's SoCs. As the industry moves to more advanced process nodes and multi-die solutions, a comprehensive approach to system-level design and performance analysis is vital.

Disaggregation is also occurring within the industry. Because commercial IP providers are selling silicon-qualified IP, many companies are choosing to outsource their IP development to enjoy cost savings and potential risk reduction. Commercially available memory compilers offer a wide range of options to enable chip designers to deploy multiple power management schemes or adjust threshold voltage implants to offset leakage. But what happens as the chip design progresses and the target specifications cannot be met? The design may cost more to complete—it may be a larger die size, it may take many more resources to close on the power-performance-area (PPA) specification, or it may require a different package because the power budget was not met.

It is highly likely that one or more memories in a chip will require some modification to meet PPA targets. This paper offers approaches to analyze memory IP and determine optimization strategies to close the gap between the design specification and design implementation in TSMC's advanced technology nodes.

Custom IC design still offers the best solution for power, cost and performance. It isn't just about getting the highest performance anymore. It's about getting the desired performance at the optimized power and area, on time and on budget. This requires many combinations and permutations that increase exponentially for complex custom ICs. It is imperative that the design team has deep silicon knowledge and up-to-date experience to make the right choices.

The paper will analyze large memory subsystems in two designs for optimization to reduce area and power without compromising performance on TSMC's advanced process nodes.

1. The first design has 536 unique memories with 3310 memory instances occupying 40 mm². The total die area is 64mm². This design includes two ARM Cortex A9 processors running at 1.2GHz under worst-case conditions on TSMC 40LP technology. When looking at potential die size reduction, a very likely candidate will be the memory content of the chip, because the memories are comprised of four different memory architectures and comprise such a large portion of the die. The most straightforward approach is to analyze the memory array efficiency. The memory content was analyzed by looking at the instances making the largest area contribution and assessing their array inefficiency (how far do they deviate from the ideal array efficiency factor). The memory area may be improved by removing unnecessary features. It is possible to customize these instances and remove the circuitry. It is also possible to reduce area by removing some of the additional margin in the tiled compiler circuitry drive strengths. The combination of these two approaches results in an area reduction of 9.97 percent in this design while still achieving the 1.2GHz performance and slightly reducing the dynamic power.

2. The second design requires a reduction of static and dynamic power for its 420Mb memory subsystem in TSMC 28HPM technology. The most obvious approach to power reduction is to reduce the operating voltage. Another approach to minimizing power is to study the effect of the threshold voltage implant under different characterization conditions. TSMC offers multiple transistor threshold implants as well as multiple operating voltages. Several approaches of varying threshold implants and operating voltages will be presented to show the most power-efficient memory subsystem.

Truly Differentiated Memory Subsystems on TSMC's Advanced Technology Nodes

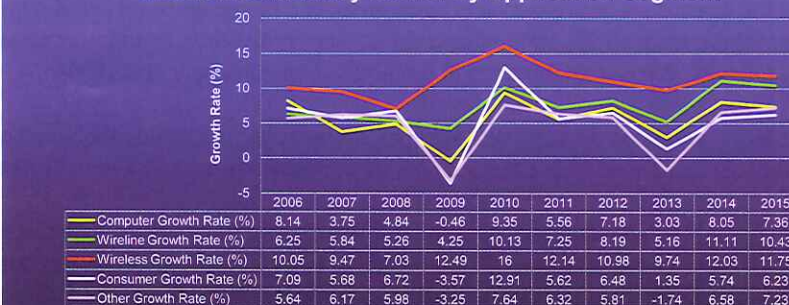


Lisa Minwell
Sr. Director IP Solutions Marketing

Electronic IC Market Dynamics



Electronics Industry Market By Application Segment



Source: IBS 2011

- The high-growth segment of the electronics industry is in wireless communications
- Wireline communications is also growing to support the increased bandwidth driven by the increased volume of smartphones, tablets, etc

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Keys to ASIC Success



- Establish close design implementation relationships with customers
- Develop the specialty IP needed for high-growth applications
- Differentiate with design expertise and IP portfolios
 - Embed large memory blocks with high-performance interfaces
 - High speed memory solutions



Source: IBS Q2 2011

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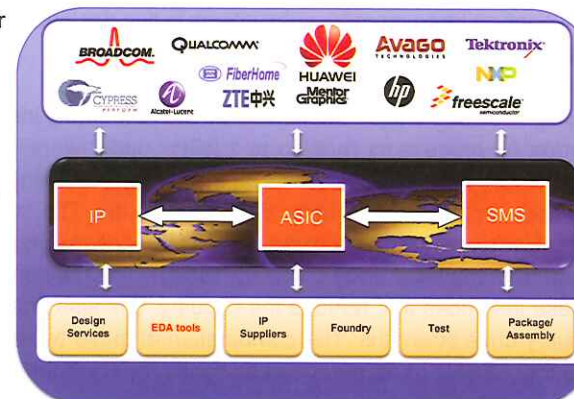
The Right Chip with eSilicon



Customer Sample

eSilicon

Supply Chain



IP Business Solutions Group
• Custom IP to optimize your chip's performance, power and area

ASIC Business Solutions Group
• Unique methodology, custom IP, and production management excellence to deliver your optimized chip

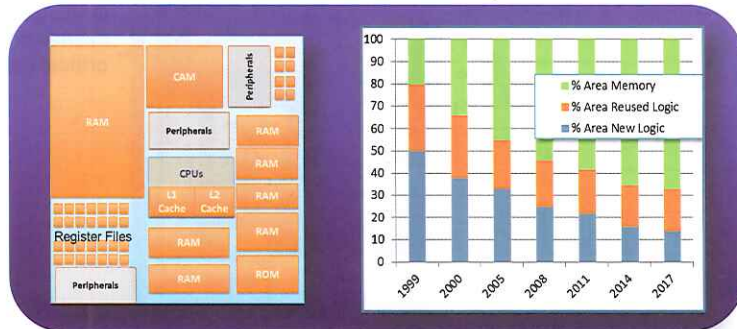
Silicon Manufacturing Services (SMS) Solutions Group
• Packaging, quality, foundry and test engineering to manage your chip in volume

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Differentiating with Optimized Memory IP



- In most new tape outs, memory encompasses >60% of the chip area
 - Dominates chip floor plan
 - Significantly impacts power, performance and area (PPA)
 - Impacts manufacturing yield



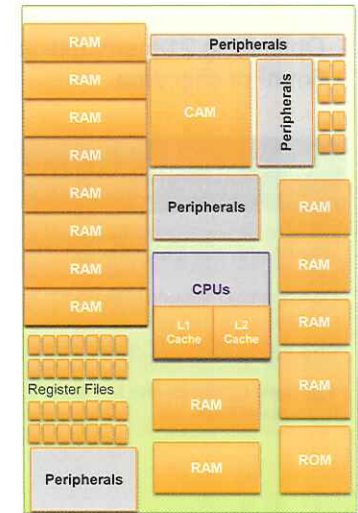
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ASIC Example – DTV



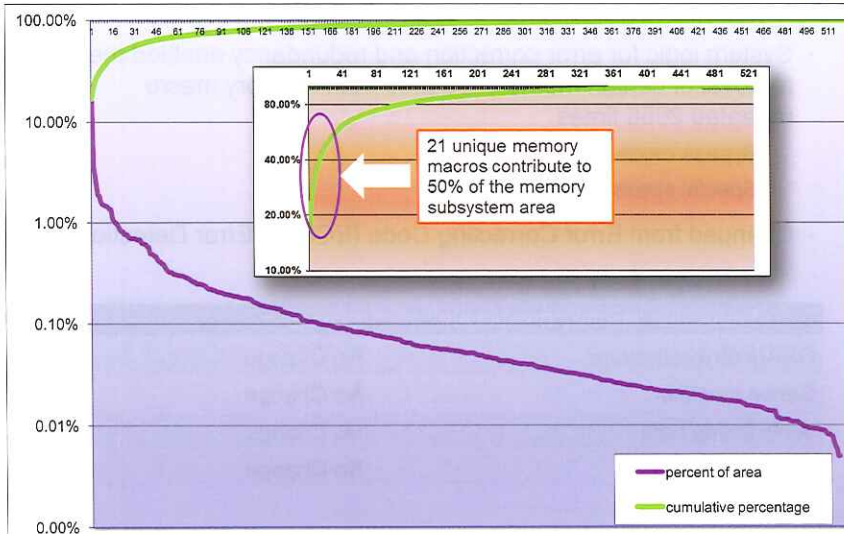
- Digital TV
- TSMC CLN40LP Technology

- 40% chip area occupied with memory
- 2,577 memory instances with 525 unique instances
- Differentiate by reducing area and power



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ASIC Example – DTV Analyzing the Memory Subsystem

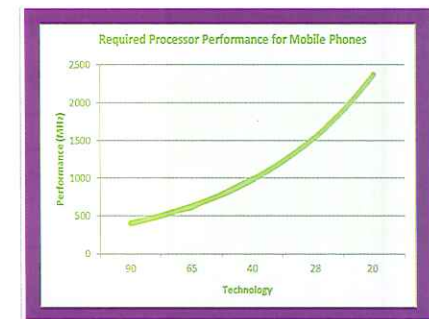


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ASIC Example – DTV Cache Optimization



- Low cost mobile products with medium performance (500MHz)
 - Improve area with the same performance in L1 cache
 - High density bit cell
 - Mixture of standard and high Vt transistors
 - Remove unused options based on system architecture
 - Consolidate large (8Mb) L2 cache
 - Replace 250 instances of 1K x 32 memory macro with one 8Mb macro
 - High Density 6T bit cell



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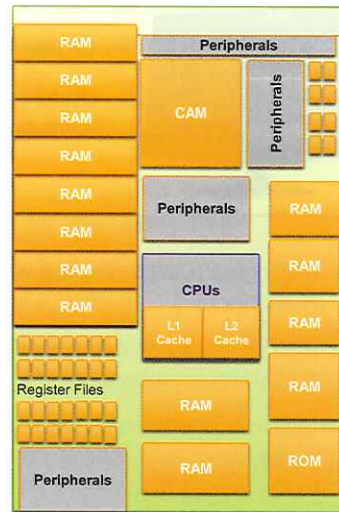
ASIC Example – DTV

Differentiating with Reduced Area and Power



- Optimizing 21 memories saves 5mm² of chip area

Area Reduction Techniques For Customized Macros	Area Reduction (mm ²)
Optimize circuits & layout for the specific array size & timing target	0.8
De-feature by removing unwanted circuitry	1.7
Changing to smaller bit cells	0.5
Aggregate L2 caches into 1 large/dense RAM	2.0

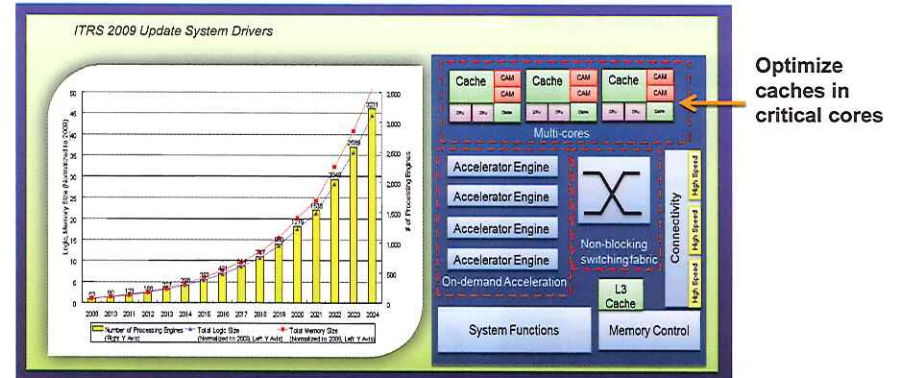


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Wireline Communications Drive Performance and Bandwidth

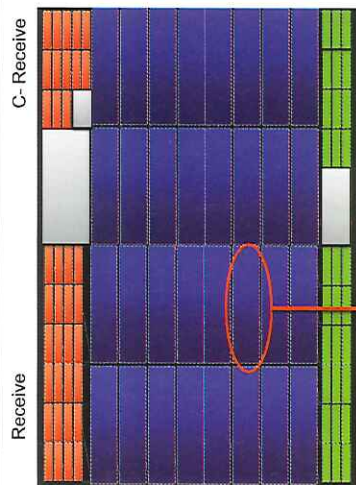


- The number of embedded processors per chip is growing and the performance is improving 1.5X per technology
 - 20nm networking system performance is >20X (with 80+ cores) the system performance of an 8-core 45nm design

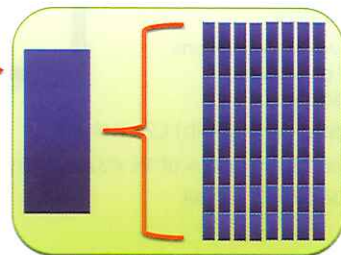


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ASIC Example – Network Processor



- CLN28HPM Technology
- 55% of the chip area is memory
 - ~450Mb SRAM
 - ~430Mb comprised of the same instance repeated 2056 times



Differentiate by optimizing key memory macro

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ASIC Example – Network Processor

Reducing Area



- System logic for error correction and redundancy enabled the removal of certain memory features from memory macro repeated 2056 times
 - Bypass mode
 - Special stress logic
- Changed from Error Correcting Code (ECC) to Error Detection

Embedded Memory Component	Change
SRAM array structure	No Change
Sense amplifier	No Change
Write timing path	No Change
Read timing path	No Change

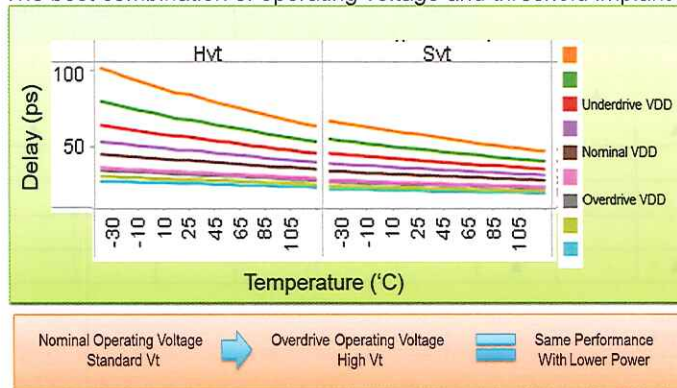
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Reduce Power

Leveraging Process Technology Features



- TSMC 28nm technologies
 - Include multiple transistor threshold implants – HVt, SVt, LVt etc.
 - Include nominal and overdrive operating conditions
- The best combination of operating voltage and threshold implant is not obvious



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ASIC Example – Network Processor

Reducing Power at the Same Performance



- Technology: TSMC 28HPM
- 394Mb memory subsystem
- Customization
 - Standard Vt memory array operated at nominal VDD
 - Migrated memory peripheral logic to high Vt
 - Re-characterized for overdrive operating voltage

- Result = Same Performance
- Static Power Savings = 20%

Architecture	Array Leakage (mW)	Periphery Leakage (mW)	Total Leakage (mW)	Array Leakage (mW) Overdrive	Periphery Leakage (mW) Overdrive	Total Leakage (mW) Overdrive	Memory Array at VDD
DP SRAM	231	3726	3957	304	2844	3075	Memory Periphery: Nominal VDD with SVt = 21 Watts
2P RF	2653	12117	14770	2769	9250	11903	Nominal VDD with HVt = 16.7 Watts
SP SRAM	262	1966	2227	313	1500	1762	FF/1.1* VDD and 1.2*VDD/125°C

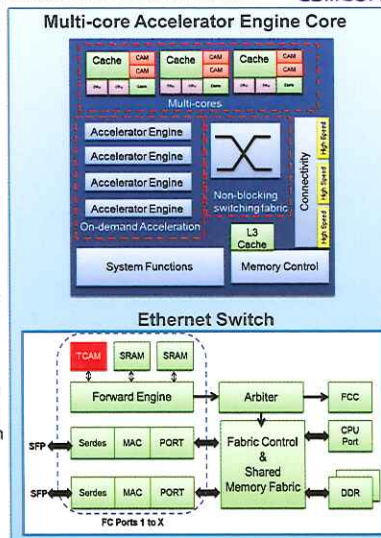
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Differentiating Intellectual Property for Networking

Content Addressable Memory



- Multi-core architectures allow power savings as well as the use of redundancy to improve manufacturing yield
 - Content Addressable Memory (CAM) can be used as a co-processor for the network processing unit (NPU) to offload the table lookup tasks
- Associative lookup structures lie at the heart of many computing problems
 - CAMs provide fast constant time lookups over a large array of data (content keys) using dedicated parallel match circuitry
 - CAMs provide a performance advantage over conventional RAM-based memory search algorithms by comparing the desired information against the pre-stored entries simultaneously. This results in an order of magnitude reduction in search time.
 - Software methods for table lookup such as radix trees are relatively slow, and they do not scale well with the table size. Under good conditions, a hash function can perform the lookup in one memory access. However, its worst-case search time, which depends on the table size and the hashing function, can be considerably worse than the tree searches.



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Unique Memory Architectures as Differentiators

Pseudo Multi-ports



- Multi-port register file
 - Increases system bandwidth by supporting parallel operations
 - Memory cell size grows quadratically with the total number of ports due to wordline and bitline writing
 - Reducing the number of physical access ports in a memory cell can thus lead to significant area and power savings as well as latency improvement
- Double-pumped multi-port register files
 - Operate access ports twice in a single clock period to reduce area by halving the number of physical ports in the memory cell
 - Replication of a memory cell in separate arrays halves the number of physical read ports in each copy

Topology	2-Port RF Cell	4-Port 4R2W Cell	Pseudo 4-Port 2x2R1W Cell
Cell Area	1X		
Read Operation	Single-pumped	Single-pumped	Single-pumped
Write Operation	Single-pumped	Single-pumped	Double-pumped

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New Specialized Memories Available at TSMC 40G and 28HPM Technologies



40LP and 28LP releases planned

CAMs are composed of conventional SRAM semiconductor memory added comparison circuitry that enable a search operation to complete in a single clock cycle

Ternary CAM

- Compiler and Macros
- Specialized bit cell to reduce area and power
- TSMC 40G: 740 million searches per second (MSPS)
- TSMC 28HPM: 850 MSPS
- Silicon proven (TSMC Memory9000™ pending)

4- Port Register File

- Compiler
- Increases system bandwidth by supporting parallel operations
- Supports 2 independent READs and 2 independent WRITES
- 4 clocks enable four operations at varying frequencies
- Silicon proven (TSMC Memory9000™ pending)

2- Port Async Register File

- Compiler
- Two Independent Write and Read ports
- Asynchronous READ enables fast access time for downstream operation
- Silicon proven (TSMC Memory9000™ pending)

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eSilicon Memories Developed for TSMC Process Technologies



Process	Foundation Memories			Specialty Memories					
	High Density SP SRAM	2-Port Register File	Via ROM	Async 2-Port Register File	Pseudo 2-Port Register File	TCAM	4-Port Register File	High Speed SP SRAM	High Speed DP SRAM
20nm SOC		▲				▲	▲	▲	▲
28nm HPM		▲		▲	▲	▲	▲	▲	▲
40nm G	▲		▲			▲	▲	▲	▲
40nm LP						▲			
65nm GP						▲	▲		
65nm LP						▲			
180nm LL	▲		▲						

▲ In Production
▲ In Development

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Summary



- eSilicon and TSMC offer truly differentiated memory subsystems by
 - Establishing close design implementation relationships with customers
 - Helping customers achieve key benefits by identifying special IP (memory) optimization that may not be obvious
 - Die or cost savings by optimizing chip area
 - Meeting challenging static and dynamic power specs
 - Achieving ultra high performance requirements needed by processor cores
 - Meeting key feature requirements of networking chips with special memories (TCAMs, multi port RFs, etc...)

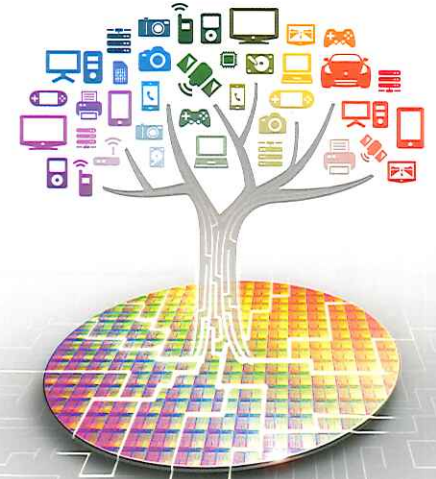
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NOTE

This image shows a single sheet of white paper with horizontal ruling lines. The lines are evenly spaced and run across the width of the page. There are no margins, text, or other markings on the paper.

TSMC 2012 Open Innovation Platform® Ecosystem Forum

The Trusted Technology and Capacity Provider



Publishing Innovation through IP Targeting TSMC Technology

Design & Reuse

ABSTRACT

D&R present its experience in how to organize a (TSMC centric) user community around a web portal in an innovative and efficient way.

How this benefit TSMC customer

One of the prerequisites when selecting a foundry process node for a SoC project is the availability of a high quality IP portfolio provided by TSMC and the worldwide IP provider community .Indeed, IPs listings demonstrate what can be achieved on TSMC process nodes at each instant by highly skilled designers . Moreover at a given time a strategic block for a customer for delivering on time an innovative Asic on the market can be found by D&R innovation tracking portal.

If TSMC can deliver info about hardened IPs as well as information of the current development of their IP partner providers ,D&R delivers a broader perspective view of all players worldwide not yet TSMC IP partner provider . It is important for TSMC customers for facing competition that innovation especially on strategic process node designs are searched and identified in real time all over the world .It is D&R mission to provide to TSMC customers real time updated comprehensive information about innovative skilled IP providers worldwide including their vision and planning . Note also that some IDM or defense companies are asking to D&R to have such DB inside their firewall to be able to follow up design innovation and this is a strategic service that DR provides.

Overall D&R is an important marketing weapon for triggering more and new designs on TSMC technology and the statistic data analysis provided by D&R gives an unique vision about market interest and evolution.

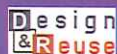
How D&R become the important IP portal that SOC designers will use for querying IP status?

Asic Designers and project managers targeting TSMC technology have to make early decision about using an external IP or developing a block themselves . Unreliable data may be a big loss for project managers as they may expect an advanced high quality IP and will not be able to have such a block ready on time for their project .Therefore D&R creates a new satellite <http://www.dr-embedded.com/foundries/> verifying the maturity and following up erroneous claims . A traffic close to 1 million of visitors is the proof that TSMC customers need such a portal .Statistics delivered ot TSMC within an annual contract gives to TSMC a real time view on the IP market interest and offer.

Publishing Innovation through IP Targeting TSMC Technology

Gabrièle Saucier

CEO
Design and Reuse



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Outline

■ Introduction

■ Innovation and acquisition

■ What's the market looking for

■ And next :D&R new initiatives

- Reliable IP maturity publishing



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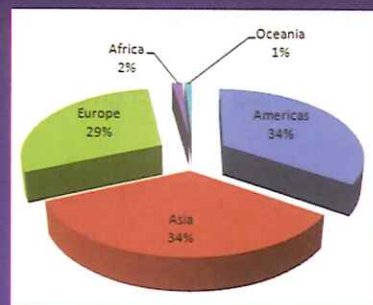
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D&R Web Site

www.design-reuse.com was created in '97 as a Market Place for (Silicon) IPs
From '97 to '00 : most of the numbers grow and *then stay close to stable*

■ The IP /SoC community was born

- 15,000 daily updated IP/SoC products descriptions
- 35,000 registered members
- 70,000 absolute unique visitors per month (source: Google Analytics)
- Asia and Far East growth
- IP SoC Newsletter
- B2B market place (Wanted IP)



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IP Providers: The Innovation Providers?

Silicon IP ? Semiconductor IP? Intellectual Property?

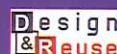
Early Vision: Core business of providers but shift

- From licensable IP providers (Star IPs) to other players: Design Center, EDA vendors, Fabless IC vendors, IDM, Foundries etc...
 - IP as catalysts of a broader product (EDA , Foundries, IC Vendors, Electronic systems ...)

■ But also researchers

- Basic devices inventors
- Software and system experts
- Mathematician, algorithmic researchers

D&R mission: Publish and report on innovation in the design area



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Innovation and Acquisition

Initially IP providers as independent providers

- Connectivity, interface IP: Standard follow up
- Analog, libraries IP based on engineering skill on new technologies
- Innovative product differentiator: application specific subsystem

Life cycle?

IP Provider/(acquisition??) /Design house/**Fabless IC Vendor/ **Systems

Increased visibility of bigger players for which IPs are catalyst

- Foundries
- iDMs ???
- Design Center
- EDA vendor
- Fabless I.C vendors and Third Party Alliance



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Innovation and acquisition

The market evolution

- Less ASIC design, exponential ASIC growth, design cost
- Market consolidation toward large companies covering vertical market segments
 - Accelerated IP provider acquisition flow
 - Predictable? How does it affect IP community?

Significant acquisitions by bigger players

- EDA vendors: Synopsys, Mentor, Cadence
- IP providers: Arm, Silicon Image
- Fabless companies: Xilinx, Altera, PMC Sierra
- Semiconductor vendors: Texas Instruments, Intel
- Apple, Google

IP provider acquisition: Best financial investment for large companies

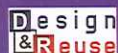
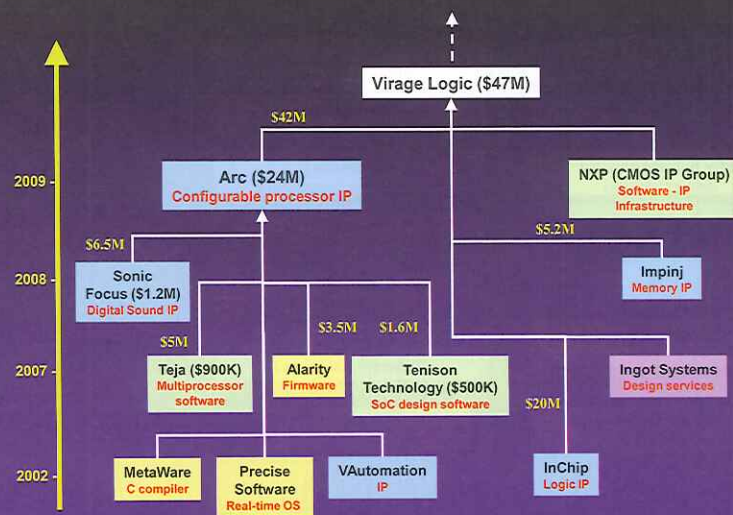


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EDA Vendor: Synopsys

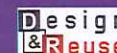
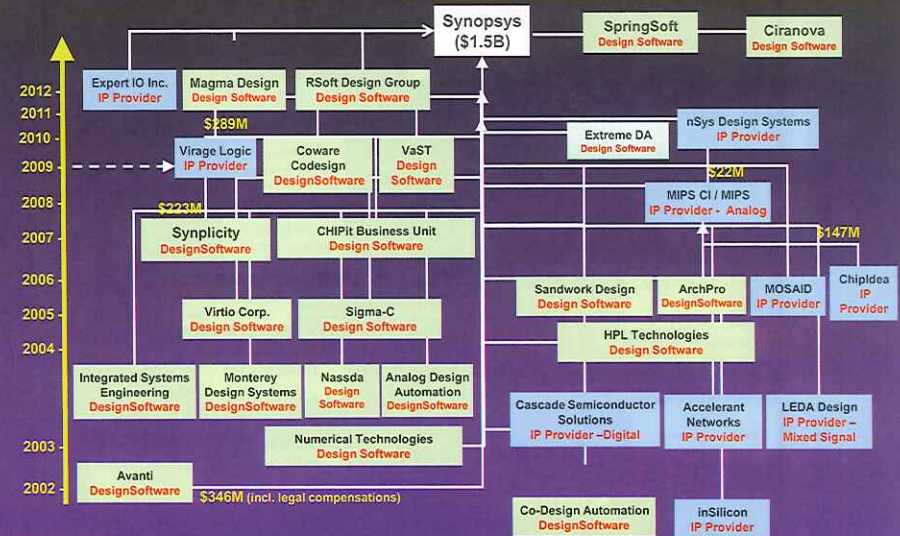


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EDA Vendor: Synopsys

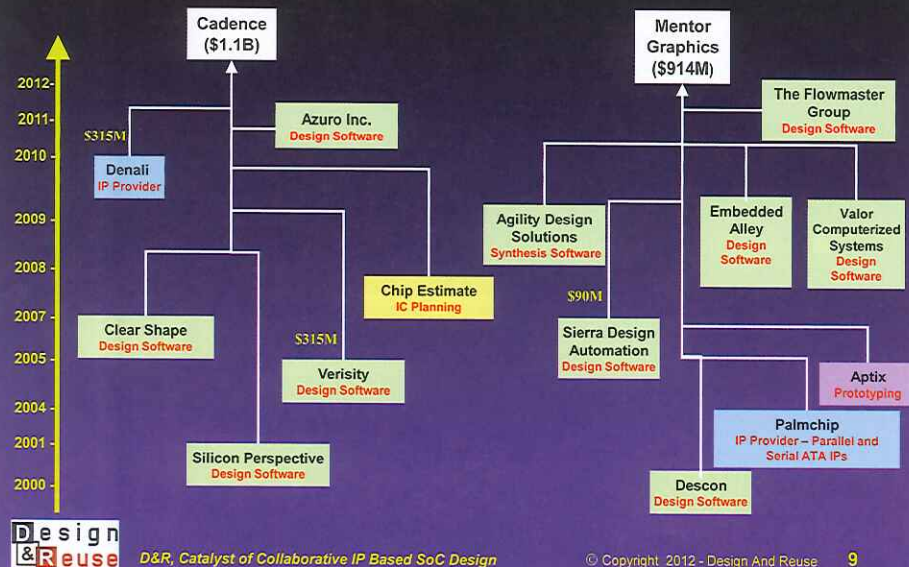


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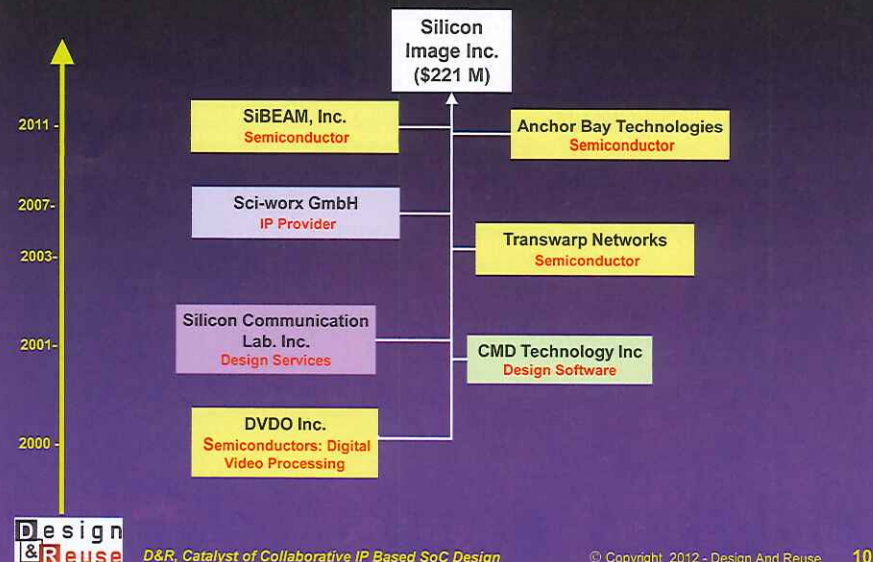
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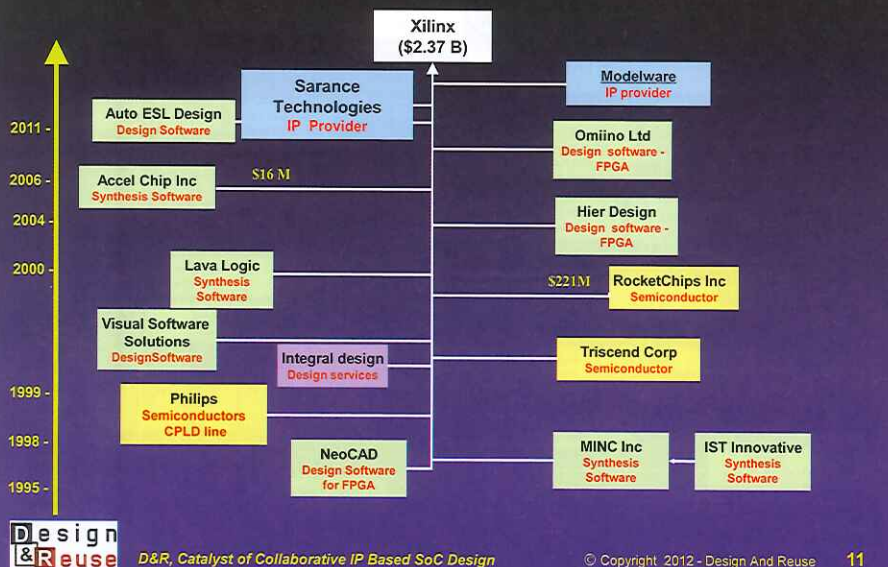
EDA Vendors: Cadence & Mentor



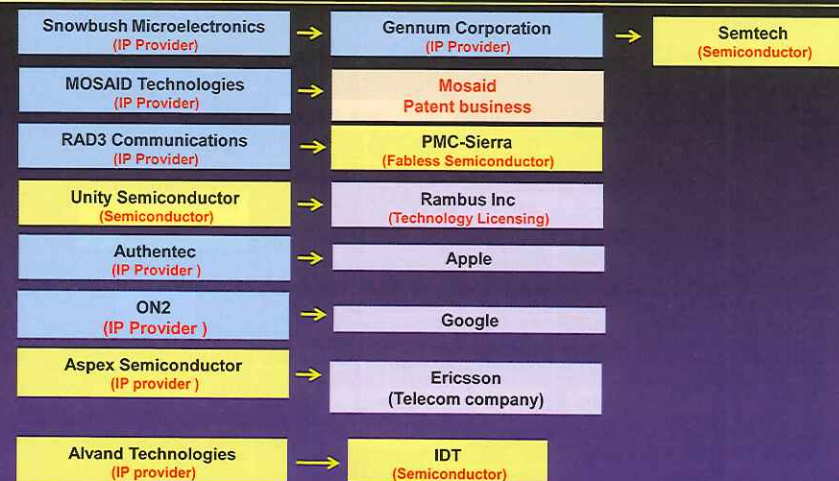
Fabless IP Vendor: Silicon Image



Fabless IC Vendor: Xilinx



Diversified Innovation Acquisition Path



What is the market looking for on TSMC target?

Updated every 6 months based on the last 12 months web site traffic

Top products

Top providers in the 4 hottest areas

- Analog & Mixed Signal
- Interfaces
- Memory
- Wireless communication

Interest of such statistics

- Analyze market trends
- IP provider selection
- Acquisition investigation

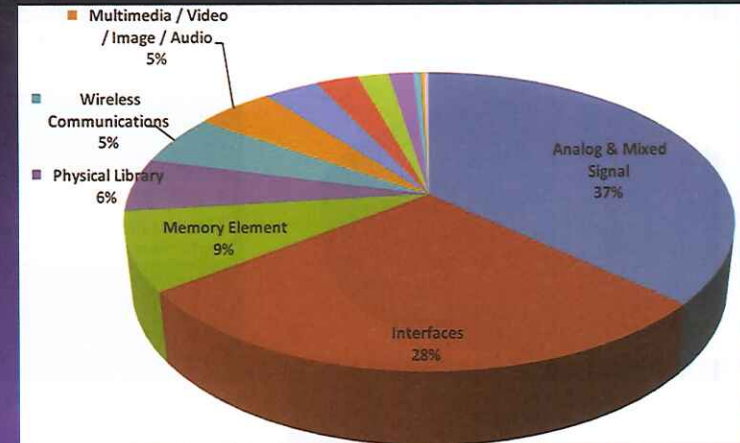


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Sector Attractiveness



Source: Statistics based on the user traffic on www.design-reuse.com Jan-Jun 2012

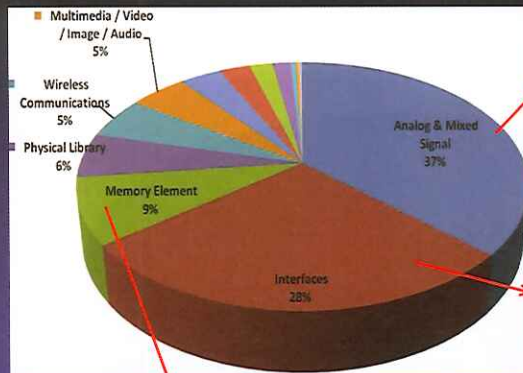


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Top Products



1. Programmable Fractional-N Frequency Synthesizer PLL (28nm - 180nm) (Silicon Creations)
2. 11-Bit 440MHz Analog Front End (AFE) (Cadence Design Systems, Inc.)
3. Ultra-Low Jitter Fractional PLL (S3 Group)

1. USB3.0 PHY (Cadence Design Systems, Inc.)
2. MIPI Compliant D-PHY (Mixel)

1. The freedom of synthesizable registers (Dolphin Integration)
2. High density, Field-Programmable OTP for eFuse, ROM and FLASH replacement in 130, 110, 90, 65 and 55nm (Sidense Corp.)

Source: Statistics based on the user traffic on www.design-reuse.com Jan-Jun 2012

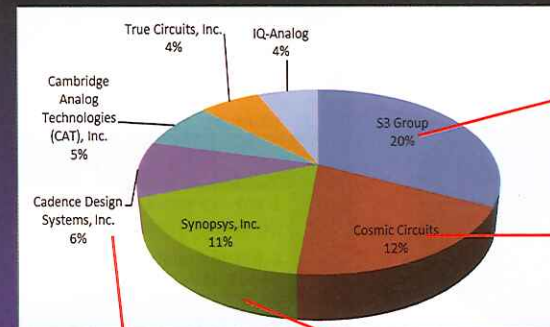


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Analog & Mixed Signal: Top Providers



1. Ultra-Low Jitter Fractional PLL
2. Power On Reset Circuit
3. 12-bit 1MS/s ADC with 4 Inputs and T-Sensor

1. 10-bit 80MSPS Dual A/D Converter
2. 12-bit 160MSPS Dual D/A Converter

1. 11-Bit 440MHz Analog Front End (AFE)
2. 14-Bit 300MHz Analog to Digital Converter

1. 12-bit, 5MSPS, 1.8V SAR ADC with Differential Input Mux in TSMC 28HPM
2. 12-bit, 250MSPS, 1.2V Wideband Pipeline IQ-ADC with 2.5V Input Buffer in TSMC 40LP

Source: Statistics based on the user traffic on www.design-reuse.com Jan-Jun 2012

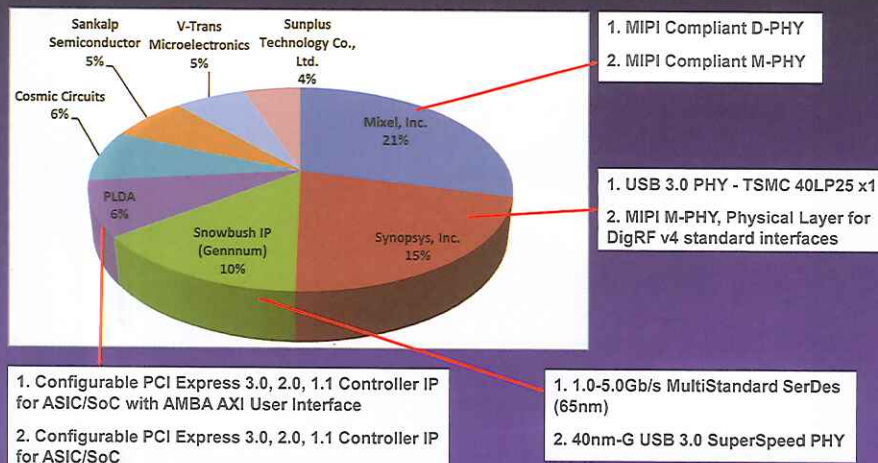


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Interfaces: Top Providers



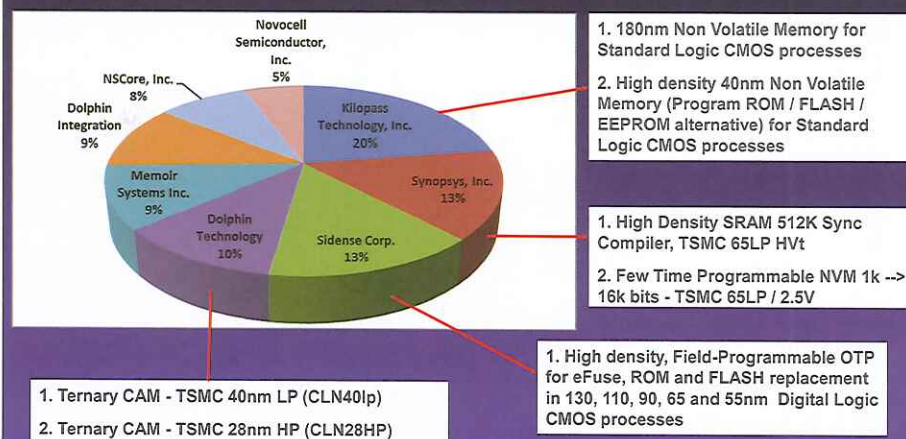
Source: Statistics based on the user traffic on www.design-reuse.com Jan-Jun 2012



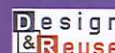
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Memory Element: Top Providers



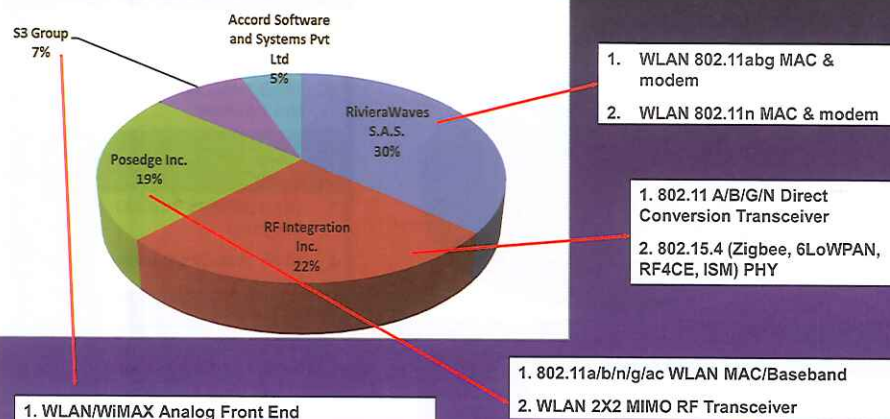
Source: Statistics based on the user traffic on www.design-reuse.com Jan-Jun 2012



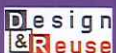
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Wireless Communication: Top Providers



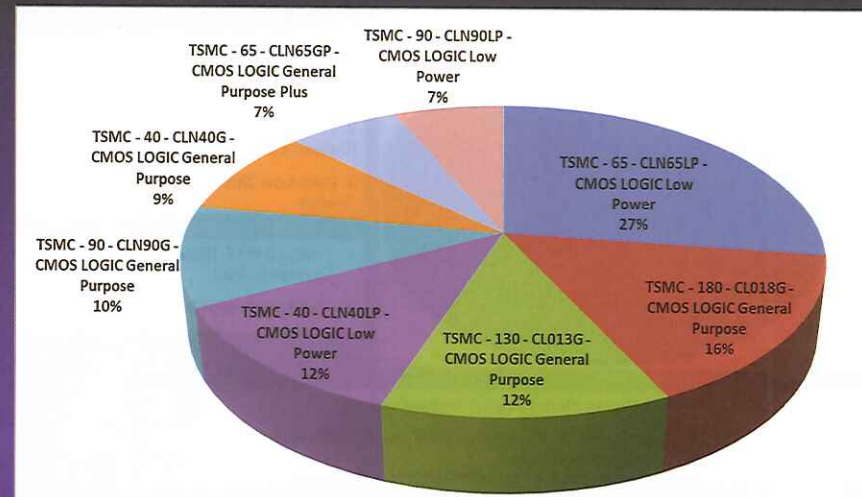
Source: Statistics based on the user traffic on www.design-reuse.com Jan-Jun 2012



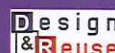
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Process Distribution of Top 8 TSMC nodes



Source: Statistics based on the user traffic on www.design-reuse.com Jan-Jun 2012



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D&R Initiative

■ ASIC Project Managers uses D&R portal (www.design-reuse.com)

- Evaluate the state of the art ,capturing innovation
- Make a fast decision if the development of a block should be triggered in house or subcontracted externally

■ Need for accurate information about the maturity of Silicon IPs on the process nodes of his ASIC

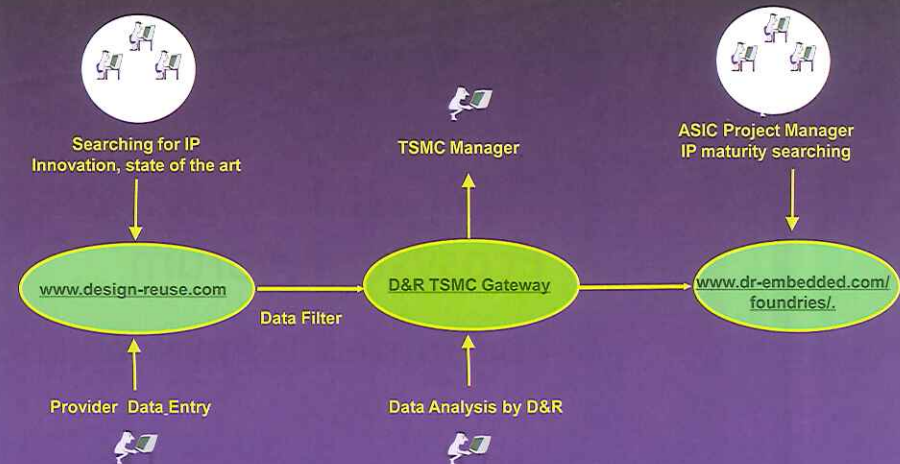
- Foundry specific information
 - Including research and future planning
 - Actors or products not yet encapsulated in TSMC program
- Maturity status
 - Pre-silicon
 - Silicon proven
 - Implemented in production design



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D&R Infrastructure for Foundry-specific Maturity Publishing



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Reliable IP Maturity Publishing

Welcome to the private page for ASIC project manager

- You are an ASIC project manager
- You really need to know which hard IP is available for your project
- D&R can investigate for you and ask for maturity assessment

Search in the Foundry Gateways

Enter Keywords: AND Operator:

Geometry nm:

Pre-Silicon:

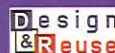
Silicon Proven:

In Production Designs:

Standard IP Maturity on Foundry process nodes

- **Pre silicon** means that your IP will be sent to Foundry within a predictable time period.
- **Silicon proven** means that at least one IP silicon implementation has been tested on the target process.
- **In Production designs** means that the IP has been used at least once in the market products.

In case of erroneous maturity claims please report to D&R. It is our



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Extended D&R Offer and Conclusion

D&R offers to providers its IP management technology to

- Create and maintain their intranet/internet IP web product catalogs
- Import export their data client intranet
- Export their data to specific portals (selective data)
- Manage their delivery
- Experienced by Dolphin integration...

Conclusion

To find Compare Evaluate Sell

Buy Manage IPs Think D&R

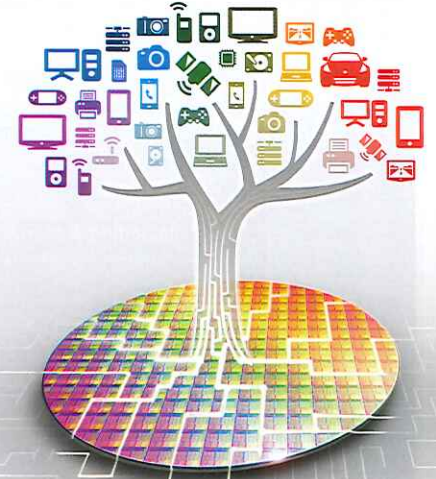


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TMI: A Unified Compact Model Development Platform for 28nm & Beyond

Synopsys & TSMC

ABSTRACT

The compact models of semiconductor devices are the bridge between design and manufacturing in the integrated circuit industry. They serve as the “contract” on transistor behaviors between IC foundries and their many customers. As such, compact models play a key role in the IC technology.

Industry standard models released by the Compact Model Council (CMC) and its university development teams have successfully served the purpose well for the above-50nm nodes. For finer geometries, they are at most “base-line” models because of the lack of the models for such complex and yet critical effects as layout-dependent mechanical stress and proximity effects, parametric variability, DFM and restricted design rules, as well as device aging and reliability. Consequently, each foundry and fab embarked on extensions to the standards in many diversified and ununified way across the industry. The impact on cost, quality, and turnaround time is therefore negative and enormous at the various stages of model development, qualification, deployment and usage at foundries, EDA companies and design companies. For 28nm and beyond technologies, the situation is even more severe. Hence, existing compact model plus macro model (sub-circuit) approach must be enhanced.

Synopsys and TSMC came forward by jointly developing an industry/CMC standard application programming interface (API), TMI, to address these challenges. TMI provides an open and unified model development platform to facilitate those advanced modeling needs. The API is constructed in C, which is much more efficient and capable than subckt syntax. TMI has been supported by all major circuit simulators and used by multiple design houses for 28nm and below.

This paper will present the design and implementation, capability of TMI, as well as the interoperation of TMI with SPICE simulators. It will first review how TMI is architected and implemented as an open, unified and standard modeling platform, from both modeling and simulation point of view. It will then illustrate in details the capabilities and applications of TMI with the examples of modeling the layout-dependent effects, MOS transistor aging modeling and analysis, and device and circuit safe-operation analysis (SOA). Comparisons with subckt-based macro models will also be made. Finally, the advantages of using TMI for foundry PDK and reference flow development and deployment will be summarized.



TMI: A Unified Compact Model Development Platform for 28nm & Beyond

Joddy Wang, Ke-Wei Su*, YC Liang*, Zhaoping Chen, Dehuang Wu, Weidong Liu, Min-Chie Jeng*, and Frank Lee
(Synopsys, Inc.; *: TSMC)

Agenda

- Background and compact modeling challenges
- TMI capabilities
- TMI design considerations
- TMI use model
- Summary

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Industry Standard Models Need Extensions

- A decade ago, Level=28 and BSIM3v3 did all
- Extensions on standards at advanced nodes
 - Layout effect models
 - Statistical models
 - DFM models
 - Aging models
- Difficult for CMC to support
 - Long time to production
 - Lack of Si data
 - Strong and complicated process dependence

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Limitations of Traditional Approaches

- Subckt-based macro modeling
 - Simulation efficiency
 - Flexibility and capability
 - Portability
- Verilog-A
 - No or difficult interfacing to C-coded models
 - Performance for transistor modeling
- Both approaches have limited capabilities on
 - MOS aging
 - Safe operating area (SOA) check
- TMI: The unified solution

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What is TMI

- TMI (TSMC Model Interface) is an API for compact model extensions
 - Higher efficiency
 - Better capability and flexibility
 - Smoother interoperability
- Applied to industry standard BSIM4, BSIM-CMG ...
- Backward compatible with existing macro models
- TMI enable model team to provide better model for advanced process technologies

TMI Development History

- 2007/Q3: TMI project initiated
- 2008/Q2: TSMC started to deploy pilot TMI models
- 2008/Q4: Collaboration with CMC API subcommittee toward standardization.
- 2009/Q3: Added MOS aging
- 2010/Q4: TMI became CMC standard
- 2011~: Further development

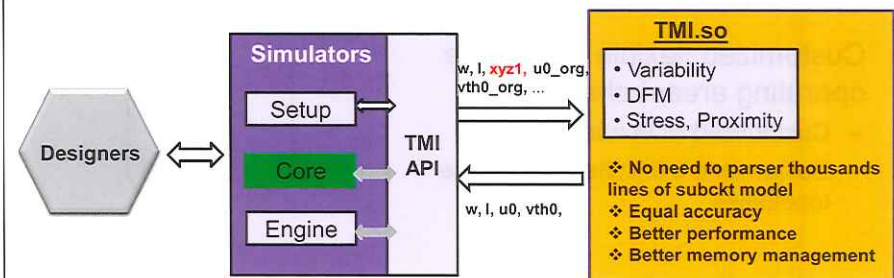
TMI production model developed for 28/20nm and below

TMI Capabilities

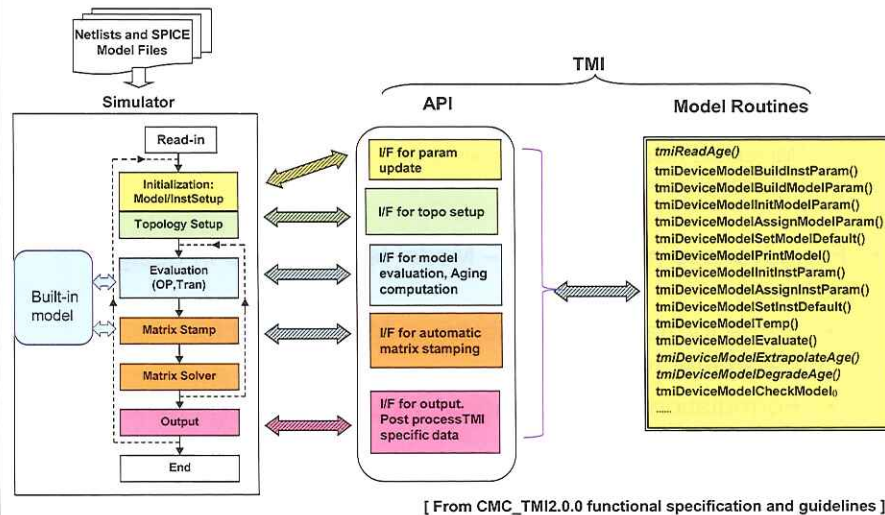
- LDE, DFM, statistical and parametric variability
- MOS aging
- Standard model topology extensions
 - Bias dependent and bias-independent components
- Additional TSMC Modeling requirements

LDE, DFM and Statistical Modeling

- User defined parameters and formulations
- More flexibility, eg.
 - Look-up table for complicated device behaviors.
 - Pre-layout LDE estimation



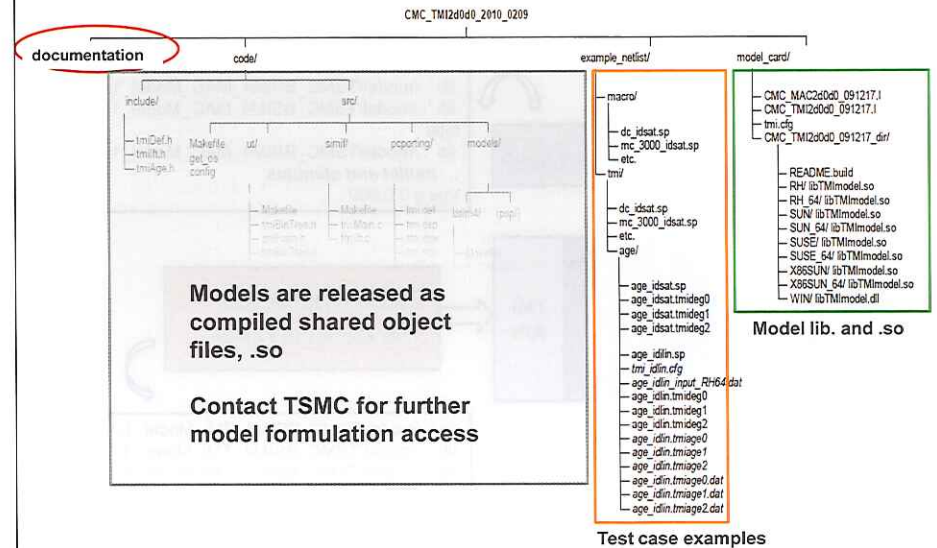
TMI Architecture and Implementation



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TMI Release Package Example



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TSMC and EDA Vendors collaborate on TMI Readiness

- Unified TMI model format.
 - No translation for specific vendor required
 - Exceptional tool specific settings or options added through collaboration between vendor and TSMC

Test environment

Date	8/15/2011
Simulator Version	HSPICE 2011.09
Package	TMI2.0.0.1_2011_0815

Platform	
RH22	v
RH64	v
SUSE32	v
SUSE64	v
SUN32	v
SUN64	v
X862UN32	v
X862UN64	v
WIN32	v

Summary of results

CMC_TMI2.0.0.1_Phase1_1-CMC-TMI_QA_comparison

File Name	Extension	Comparison
### A_e_1_nch_iboff	tout	- PASS
### A_e_1_nch_idlin	tout	- PASS
### A_e_1_nch_idsat	tout	- PASS
### A_e_1_nch_lobf	tout	- PASS
### A_e_1_nch_lobf	tout	- PASS
### A_e_1_nch_vth_lin	tout	- PASS
### A_e_1_nch_vth_sat	tout	- PASS
### A_e_1_pch_iboff	tout	- PASS
### A_e_1_pch_idlin	tout	- PASS
### A_e_1_pch_idsat	tout	- PASS

- Comprehensive QA suite for tool validation
 - Features
 - Accuracy and performance
 - Outputs, Error/warning message
 - Version control
 -
- Simulator automatically detect OS and select the right TMI

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Macro and TMI Model Card Comparison

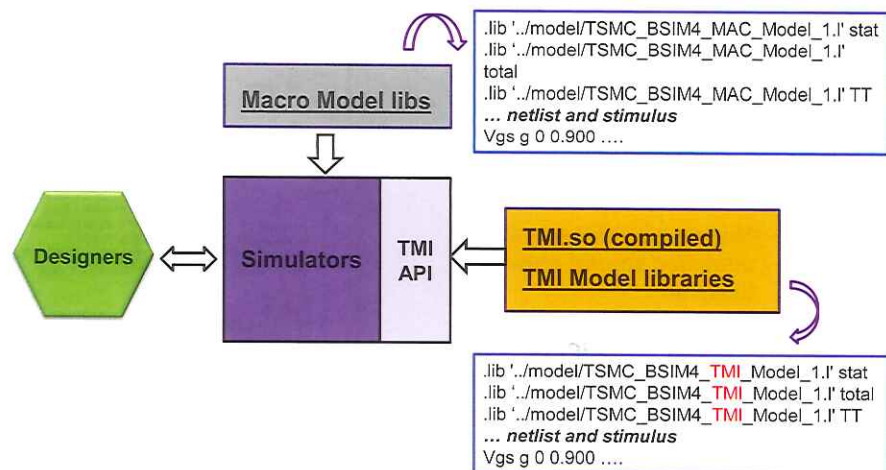
```
* File : TSMC_BSIM4_MAC_Model_1.I
* Date : 2012_0626
* Description : BSIM4 macro sample model
* MODEL : BSIM4 4.5
.LIB setup
.param ccoflag=0
...
.ENDL
.LIB stat
...
.LIB ttg
...
.LIB Total
.subckt nch_mac n1 n2 n3 n4 l=length w=width
multi='1' nf='1' scale='scale_mos'
+ _dmog='2.2e-8' ....
main n1 n2 n3 n4 nch w=ww l=ll ...
.model nch.1nmos level=54 ... BSIM4 parameters
.ENDL
```

```
* File : TSMC_BSIM4_TMI_Model_1.I
* Date : 2012_0626
* Description : BSIM4 TMI sample model
* MODEL : BSIM4 4.5
.LIB setup
.option tmiiflag=2.01 modmonte=1 tmiptm='TSMC_BSIM4_TMI_Model_1_dir'
.lib 'TSMC_BSIM4_TMI_Model_1.I' setup_age
.param ccoflag=0 ....
.ENDL
.LIB stat
...
.LIB ttg
...
.LIB Total
.LIB setup_age
.param
+dagetime = 0 age_unit = 0 phys_id = 0 r_hci = 1 r_btj = 1
.option tmiAge = 1 tmiSave = 1 tmiinput = 'tmi.cfg'
.ENDL setup_age
.LIB Total
.model nch_mac.global nmos
+modelid = 1 level = 54 version = 4.5 xyz2=
.model nch_mac.1 xyz2=... BSIM4 and TSMC specific parameters
.ENDL
```

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Switch From Macro Model to TMI is Transparent



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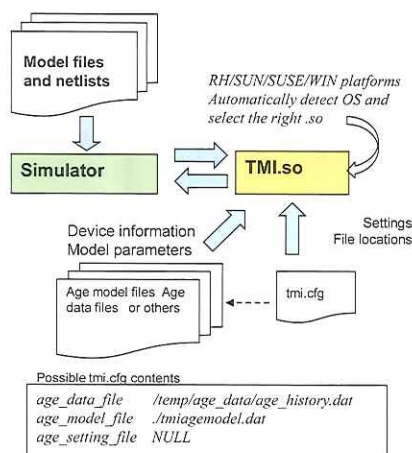
Usage Model

- For general model users
 - Same way as conventional macro model to call model library from netlist
 - Same format of model libraries
 - TMI related model settings and simulation options are made ready in TMI model libraries
- For advanced model users – Model team or CAD in design company
 - Same format of model library in ASCII format for parameter tweaking
 - Formulations in the compiled TMI.so can be requested from TSMC
- Same support model from EDA vendor and TSMC

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More TMI Examples

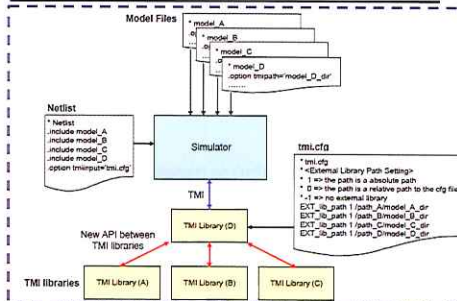


Supports many new simulation functions (age, SOA ...)

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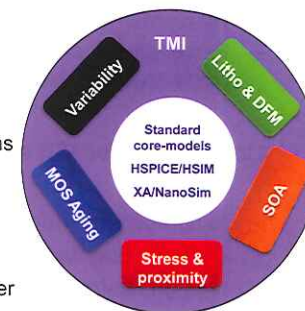
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Multiple .so for different device flavors



TMI Benefits

- Designers
 - More efficient than macro approach
 - Availability of software techniques to qualify and manage the model
 - Unified model format, Tool- Independent
- Model Providers
 - TMI enables and facilitates more model innovations
 - Flexible and capable
 - Powerful c-code flexibility and capability.
 - Possibility of complicated data structure to implement new model algorithms.
 - Access to more simulation information for better modeling.
 - Quick TAT of deployment and production
 - Transparency to existing design flows.
 - Better integration with existing tools and flows for new model functions



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Summary

- Macro model sees challenges in advanced nodes
- TSMC and Synopsys collaborated in TMI as a unified efficient solution
- Benefit of TMI
- Continue TMI future enhancements

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Design Methodology for Silicon-Accurate Jitter Analysis for 28nm Interface IP for 100GB Applications

Berkeley Design Automation & Analog Bits

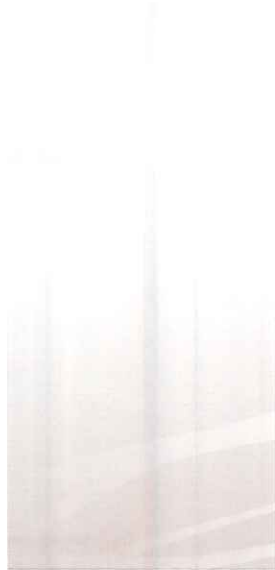
ABSTRACT

The successful design of a SerDes for 100GB Ethernet applications requires providing accurate quadrature outputs from a high-performance PLL at very low dissipated power levels. This paper describes the design and verification methodology of a 14GHz SerDes PLL for 100GB applications fabricated in TSMC 28nm technology which produces quadrature outputs and a measured output clock jitter $< 0.3\text{ps rms}$ in under 12mW of power. The circuit verification methodology used to complete the jitter analysis relies on Berkeley Design Automation Analog FastSPICE (AFS) Platform and includes analysis of all device noise contributions, sensitivity analysis, RC parasitics, PVT and mismatch variations. The AFS Platform is certified in TSMC SPICE-Qualification Program, and AFS device noise sub-flow validated in TSMC AMS Reference Flow 2.0.

In this paper, we first review the design requirements for a SerDes IP macro for 100GB Ethernet applications, the OIF-CEI-28G*specifications, and the corresponding requirements on the high-performance PLL to meet the stringent jitter specifications. We describe the key effects that must be captured in any analysis to provide an estimate of the phase noise and jitter expected in TSMC 28nm technology. These include the impact of device noise, the identification of the top noise contributors, the capture of all post-layout effects, comprehensive PVT, and mismatch analysis using the AFS Platform.

We compare the alternate methods available to analyze phase noise and jitter (both random and deterministic) and summarize the advantages and disadvantages of each method. We first begin by looking at a traditional blocklevel analysis approach, using post-layout analysis results for each of the key components and using a linear transfer function model to complete the analysis. We then look at a new full-loop simulation approach using transient noise analysis. By using a systematic approach using new characterization techniques available in the AFS Platform, we are able to achieve a fast turn-around-time to complete a comprehensive analysis.

We then present the results for phase noise and jitter analysis and illustrate the excellent results obtained via the new full-loop simulation approach using AFS Transient Noise analysis. We demonstrate phase noise results with excellent correlation to silicon measurements to within 3 dB in the frequency ranges of interest. The resulting methodology extending simulation-to-silicon correlation is now a standard practice for the development of our 28nm and 20nm interface IPs.



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Design Methodology for Silicon-Accurate Jitter Analysis for 28nm Interface IP for 100GB Applications

Alan Rogers, Nandu Bhagwan - Analog Bits
Ravi Subramanian - Berkeley Design Automation



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Introduction

- Presenting verification results of SerDes PLL IP
- Three way collaboration between:
 - Analog Bits: 28nm IP macro for 100 Gigabit Ethernet
 - TSMC: Reference flow development and 28nm process
 - BDA: Device Noise Analysis in the AFS Platform



Open Innovation Platform®



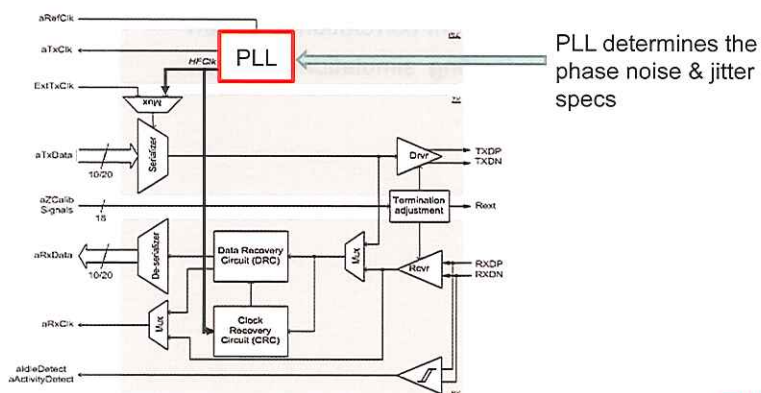
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SerDes IP Targets SoC Applications

- Multi-Rate, multi-Protocol, programmable SerDes IP
- Minimize power, latency and area (determines ring or LC)
- Stringent verification challenges (phase noise & jitter)



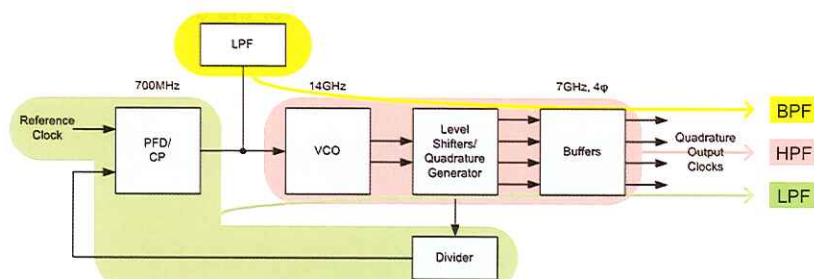
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PLL Verification Challenges

- Need to precisely analyze and predict PLL phase noise & jitter
- PLL simulations are very expensive (time & compute resources)
- Traditional SPICE simulators do not have performance and capacity
- Need full-spectrum device noise to accurately verify phase noise
- Need nanometer SPICE accuracy to predict silicon performance



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PLL Analysis Methods: Pros and Cons

Simulation Method	Architectural Block-level	Transient Noise Closed-Loop
Effective Analysis Range	Full Band	Full band (Low freq limited by runtime)
Spur Evaluation	Freq Domain: No Time Domain: Yes	Yes
Noise Modeling of RefClk, Supply, etc.	Yes	Needs to be added to netlist
Simulation Setup/Complexity	Simple	Simple
Convergence Issues	Minimal	None
Accuracy	Implementation Dependent	Nanometer SPICE
Simulation Time	Fast	Intensive for low offset frequencies

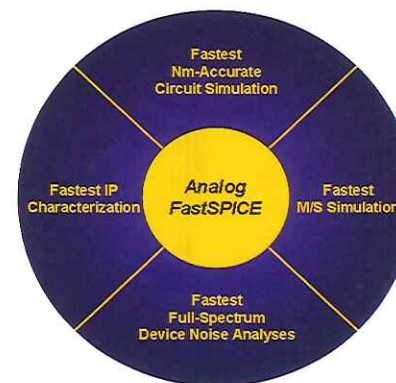


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Analog Bits Selects Analog FastSPICE™ (AFS) Platform



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AFS in TSMC AMS Reference Flow

Analog FastSPICE Transient Noise (AFS TN)

● Functionality

- Random noise for each source at each timestep
- White & flicker noise sources
- Noise based on instantaneous device bias
- Turn noise on/off at block level

● Accuracy

- Solve stochastic equations for noisy waveforms
- Advanced timestep control for random noise
- Improved tolerance settings for transient noise
- Ensures statistical accuracy for device noise
- Accurate post-processing method

● Performance and capacity

- AFS Transient is 5x-10x faster vs. traditional SPICE (1-core)
- AFS TN vs. AFS Transient <2x per timestep
- AFS TN supports AFS Multi-Core Parallel mode
- Over 10M element capacity

Analog FastSPICE Platform

Spectre or HSPICE netlists

ADE or command line

AFS Transient Analysis

Baseline sims w/o device noise

AFS Transient Noise Analysis

Device noise @ every timestep

Post-process to freq. domain

Power Spectrum, phase noise, ...

Outputs: PSF, tr0, FSDB

Compatible with most viewers

TSMC Analog Mixed-Signal Reference Flow 2.0



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AFS Device Noise Analyses (DNA)

Circuit Type	Transient Noise	Periodic Noise	Oscillator Noise
Non-Periodic Circuits			
PLLs (int-N & frac-N)	✓		
ADCs (sigma-delta, pipelined, etc.)	✓		
Tx chains & Rx chains	✓		
PHYs & SerDes	✓		
Periodic-Driven Circuits			
Switched-cap filters	✓	✓	
Mixers	✓	✓	
Phase detectors	✓	✓	
Charge pumps	✓	✓	
Dividers	✓	✓	
Periodic-Autonomous Circuits			
VCOs (LC-tank, ring oscillators)	✓		✓
Crystal oscillators (XOs)	✓		✓

Golden reference

Faster with superior diagnostics where applicable



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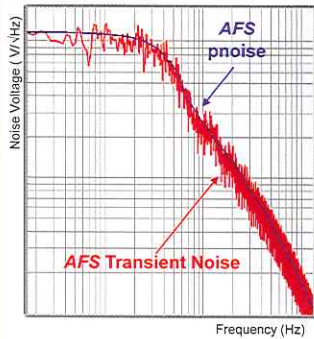


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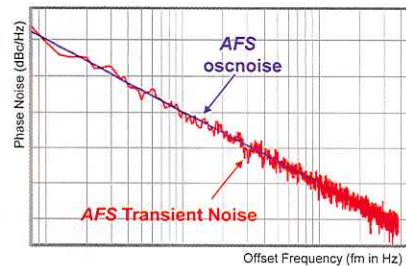
AFS TN: Full-Spectrum Correlation

Full-Spectrum Transient Noise & Periodic Noise Provide Excellent Correlation

Switched-Cap Filter Noise Comparison



4.75GHz LC VCO Noise Comparison



Industry's most accurate, fastest, highest-capacity device noise analysis



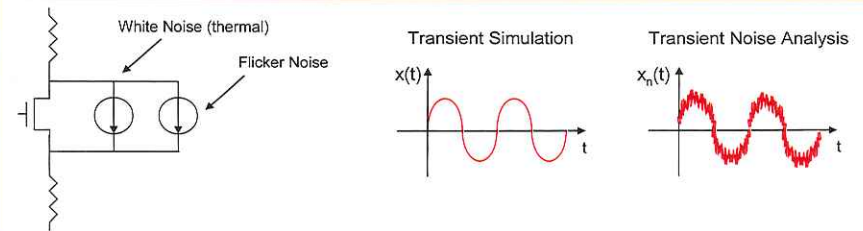
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Transient Noise (TN) Analysis



Transient Noise Analysis

- Noise for each source at each timestep
- White & flicker noise sources
- Noise based on instantaneous device bias
- Generates waveforms with representative noise
- Post-process waveforms for desired specs

Transient Noise Analysis Accuracy

- Library noise information
- Transient noise floor (SPICE tolerances)
- Number of samples (cycles)
- Post-processing method
- Validation with other methods & silicon

Only AFS solves stochastic differential equations every node every timestep



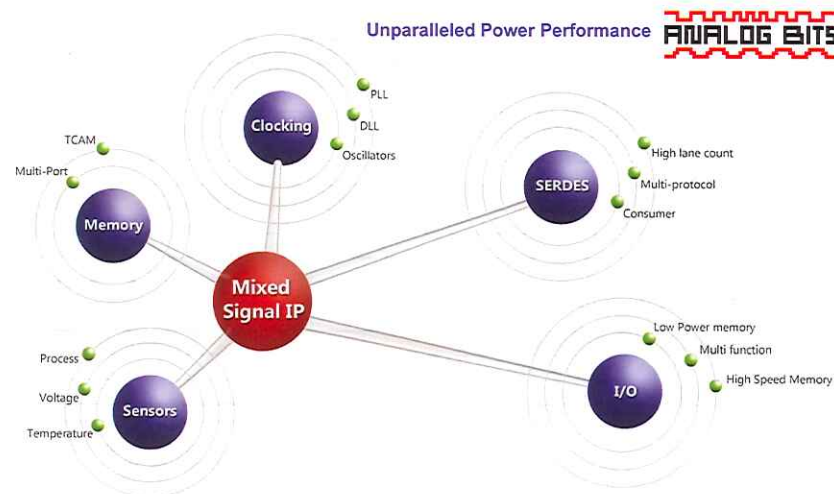
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AFS Verification of the Broadest Portfolio of Differentiated IP



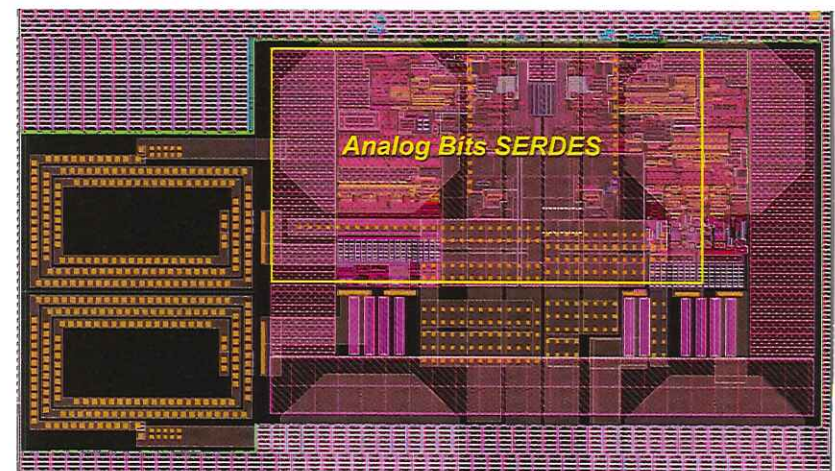
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SERDES Under a Bump Pitch



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Block Level AFS + Transfer Function Aggregation

Example of Block Level Extraction for VCO

• Circuit Inventory

bsim4v5_0	280
bsource_c	257
bsource_i	187
capacitor	203
diode	2
inductor	180
mutual inductor	6
resistor	6
vsources	50

• Analysis Conditions

	VCO 1	VCO 2
VDD	1.8V	1.2V
FOUT	13.7 – 13.8 GHz	
Conditions	SS, Lo T (0°)	
Types of Analysis	Transient Noise, OSCNOISE	

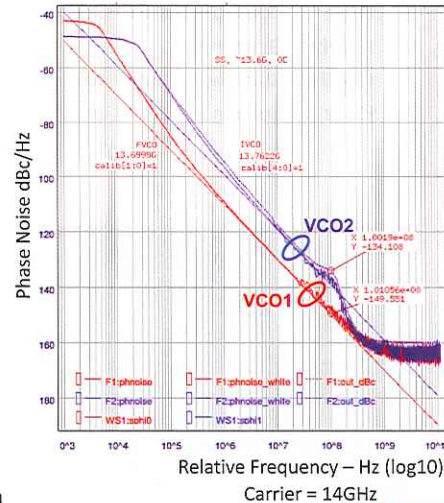
• Simulation Runtime

– 23 mins on 4 Xeon X5460 @3.16GHz CPUs

• Good OSCNOISE and AFS TN correlation



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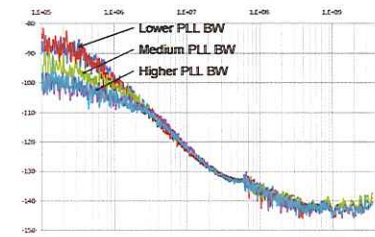
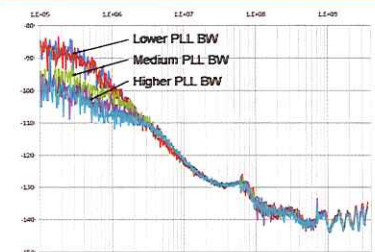


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Silicon Measurements

SS	Low Amp	Med Amp	Hi Amp
Low BW	384		373
Med BW		366	
Hi BW	333		307

FF	Low Amp	Med Amp	Hi Amp
Low BW	378		337
Med BW		360	
Hi BW	303		285



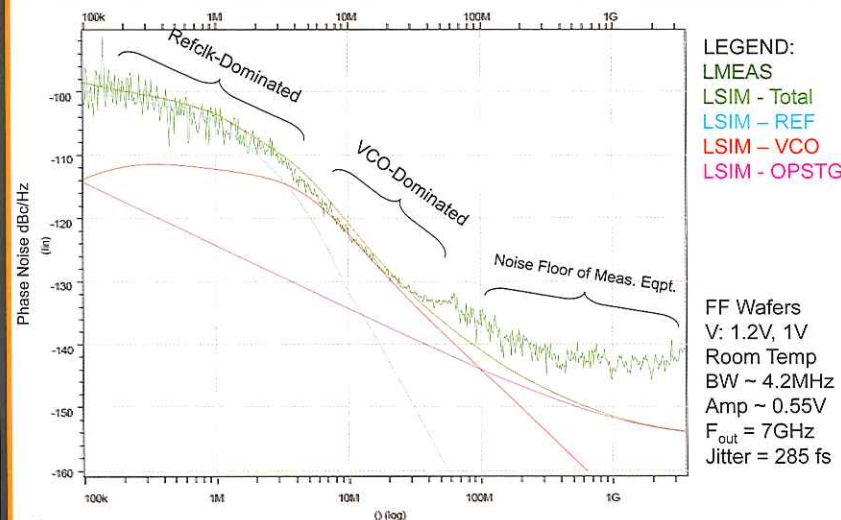
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Silicon Correlation (Best Case)

FF Wafers, High BW, High VCO Amp



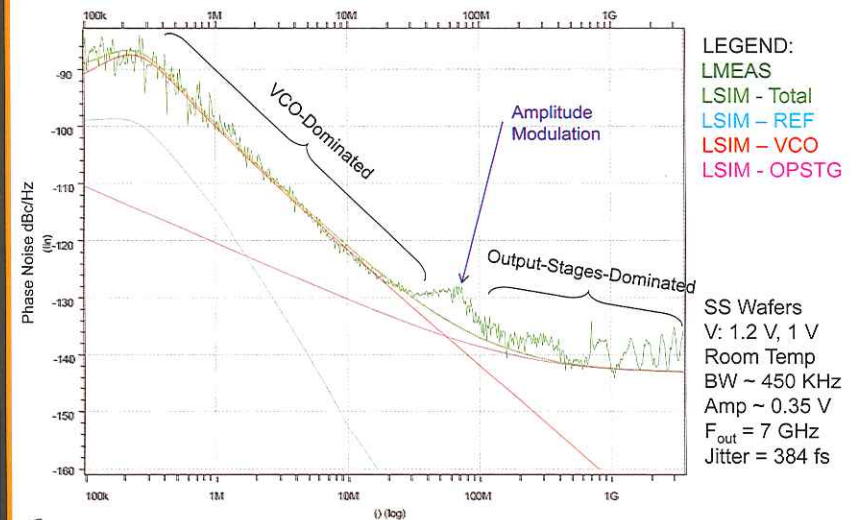
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Silicon Correlation (Worst Case)

SS Wafers, Low BW, Low VCO Amp



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Closed- Loop PLL Transient Noise Simulation

• Circuit Inventory

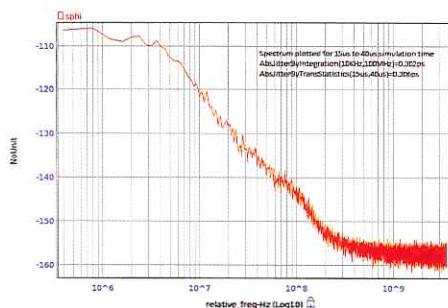
bsim4v5_0	1133
bsource_c	277
bsource_i	481
capacitor	429
inductor	196
mutual inductor	6
resistor	12
diode	40
vsources	78

• Accuracy Settings

.option reitot=1e-5 fast=2 \$ maxstep=2p delmax=2p
 .tran 2p '1024*44*tper'
 noiseifmax='14e9' noiseifmin='300e3'

• Simulation Run Time

– 11 days on 4 Xeon X5460 @3.16GHz CPUs



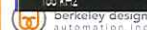
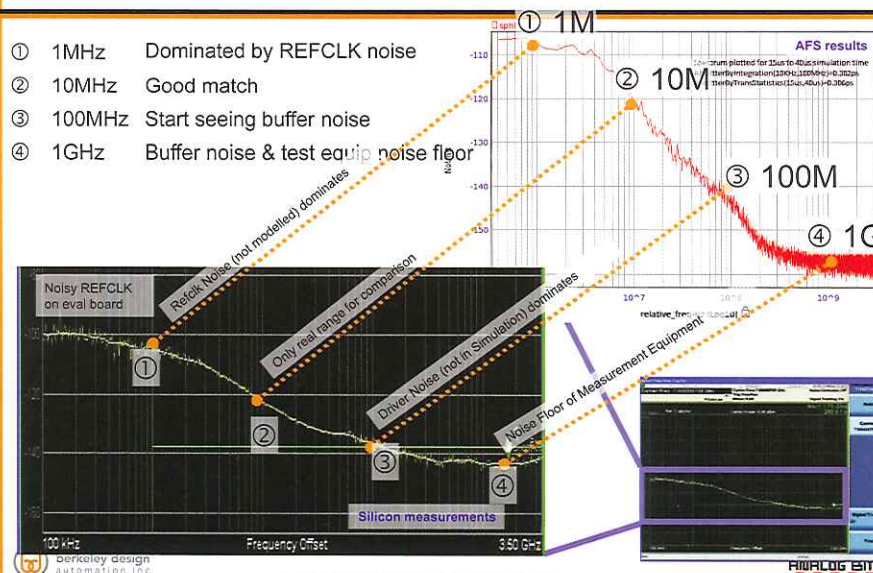
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Closed-loop Transient Noise vs. Silicon

- ① 1MHz Dominated by REFCLK noise
- ② 10MHz Good match
- ③ 100MHz Start seeing buffer noise
- ④ 1GHz Buffer noise & test equip noise floor



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Conclusions

- Lowest jitter PLL with 100 Gbps data transfer rates
- Silicon-proven in TSMC's 28nm process
- Performance characterized with AFS Platform enabling
 - Rapid and accurate block-level and top-level analysis
 - Good simulation-to-silicon correlation
 - Leveraging new full-spectrum device-noise analysis technology
 - Improved analog SerDes sign-off flow
 - Increased design productivity and reduced risk
- BDA-TSMC Device Noise Analysis Sub-flow provided good results in reasonable run-times



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Acknowledgements

- David Lee (Berkeley Design Automation)
- Mathew Parker (Berkeley Design Automation)



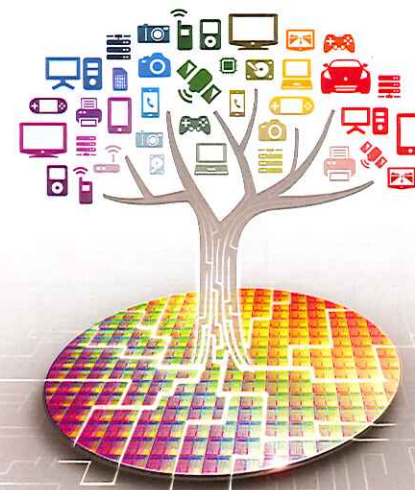
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This image shows a single sheet of white paper with horizontal ruling lines. The lines are evenly spaced and run across the width of the page. There are no margins, text, or other markings on the paper.

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Comprehensive Simulation and Modeling Solutions for TSMC's RF Platforms

Agilent / EEsof

ABSTRACT

Continuous EDA tool enhancements and new capabilities are essential for successful RFIC designs. Meanwhile, foundry and EDA collaboration are equally important to ensure silicon-accurate results at advanced RF process nodes or for novel 3D-IC integration approaches. Agilent EEsof works closely with TSMC to provide dedicated RF design flow support to address the advanced challenges of today's sophisticated RF and microwave designs. As a result, Agilent's EEsof is a main EDA partner for the 60 GHz CMOS RDK and supported in numerous RF process design kits.

The paper describes Agilent EEsof solution across different design domains from front-to-back IPD (Integrated Passive Devices) IC design implementation, to dedicated RF circuit and EM simulation solutions for large-scale RF SoCs and all integrated together in RF modules.

Various domain examples will come from dedicated collaborative efforts with TSMC, like the latest progress to provide a certified millimeter wave-ready RDK (Reference Design Kit) targeting 60-GHz application for the TSMC 65nm process and a complete front-to-back ADS PDK for TSMC's IPD 0.18 μ m process.

Comprehensive Simulation and Modeling Solutions for TSMC's RF Platforms

Dr. Juergen Hartung
RFIC Product Marketing & Foundry
Program Manager
Agilent EEsof



George Estep
RFIC Application Development Engineer
Agilent EEsof



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Agenda

- RF Design Challenges
- TSMC – Agilent collaboration examples
 - 60-GHz Reference Design Kit (RDKit)
 - IPD design enablement
- Directions & Summary

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Time-to-Market – Today's Tablets as an Example

Data

Wi-Fi® 802.11a/b/g/n
possible: 802.11ac

Location

A-GPS
possible: Galileo, Beidou, GLONASS

Personal Connectivity

Bluetooth v4.0
possible: 802.11ad/WiGIG



Communications

4G LTE
Also: LTE-Advanced, MIMO

HSPA, HSPA+

DC-HSDPA
Also: GSM/EDGE, WCDMA,
Multi-Standard Radio (MSR)

- Increasing Integration – Multiple different complex systems placed in close proximity
 - Increasing design complexity and compaction
 - Concurrent design teams across companies
 - Verification across design domains (IC/package/board)

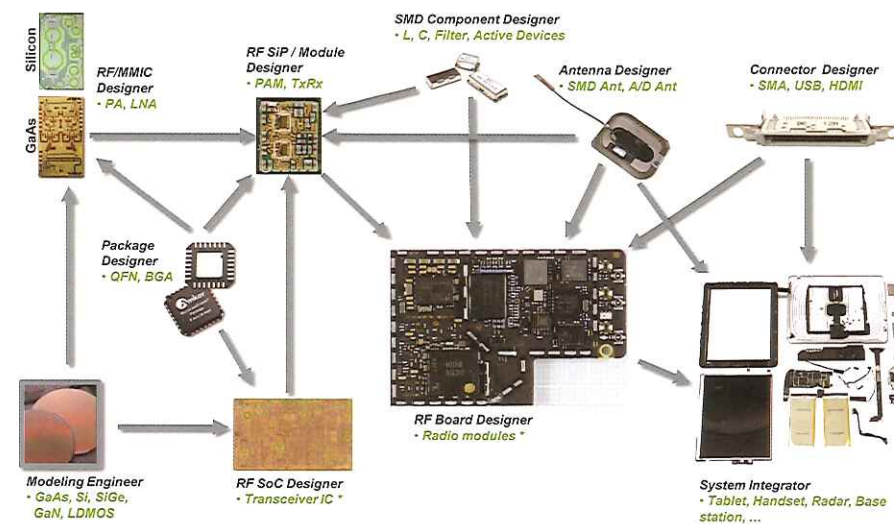
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RF/MW Design Segments



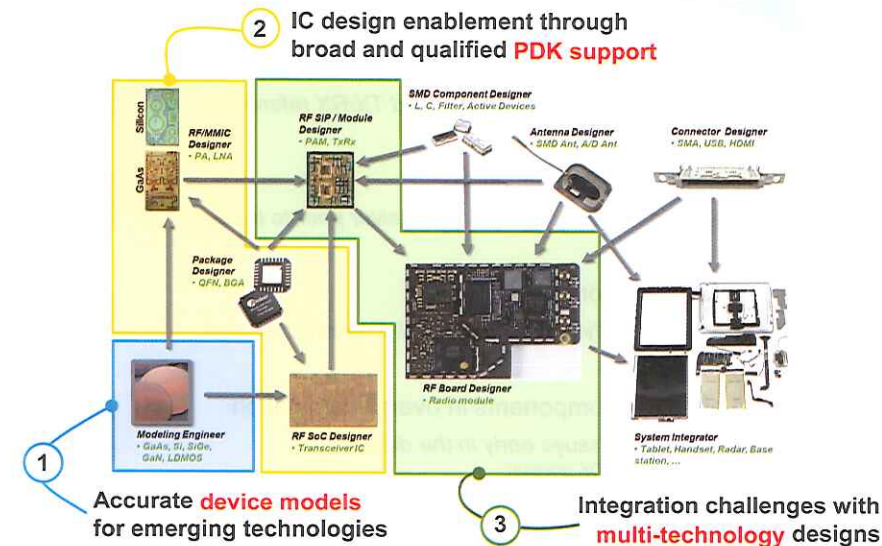
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TSMC – Agilent Collaborations: Three Main Areas



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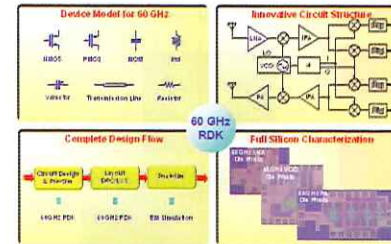
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TSMC – Agilent Collaboration: Two Examples on IC Enablement

60 GHz RDK

- RF frontend circuits (LNA, PA, and VCO)
- Achieve reliable measurement results
- Enable RF top-down design methodology to perform system level simulation with behavior model solution
- Extra devices/ transmission line support



IPD design enablement

- Integrated Passives Devices process for the production of baluns, filters, couplers, and diplexers on a separate die
- Used in RF modules & RF System-in-Packages in portable, wireless and RF applications
- Provide complete ADS front-to-back PDK

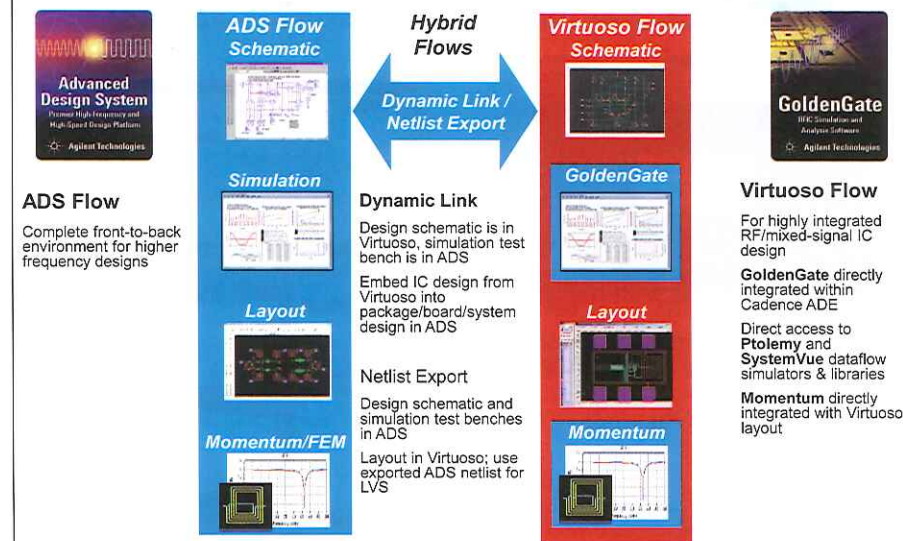


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Agilent EEsof RFIC Design Flows – Introduction



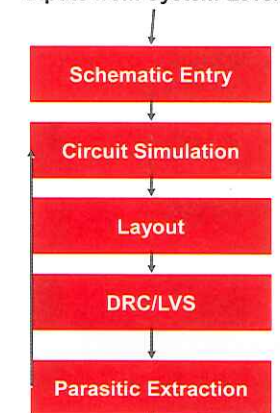
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Agilent EEsof RFIC Solutions within Virtuoso

Inputs from System Level



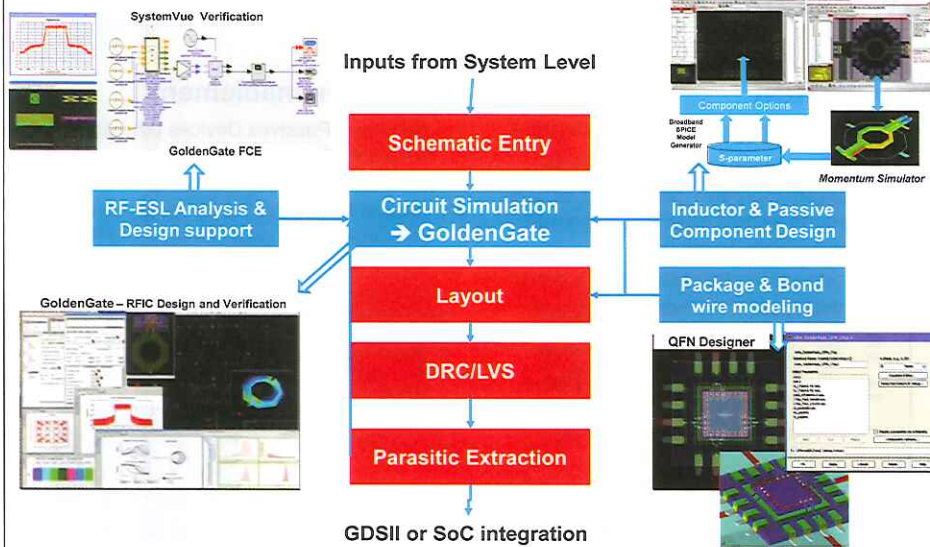
GDSII or SoC integration

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Agilent EEsof RFIC Dolutions within Virtuoso



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Solutions for TSMC's RF Platforms

Agilent EEsof 60-GHz RDK Contributions

- Top-down ESL architecture verification
 - *Verify at every level vs. consistent 802.11ad TX/RX references*
- RFIC circuit simulation & verification
 - *Full characterization of complete RF transceiver prior to tape-out*
- EM analysis & verification
 - *Enable EM analysis early and often through integrated solvers*
- Add off-chip effects & components in overall verification
 - *Addressing integration issues early in the design cycle*
(Will be added in a next RDK release)



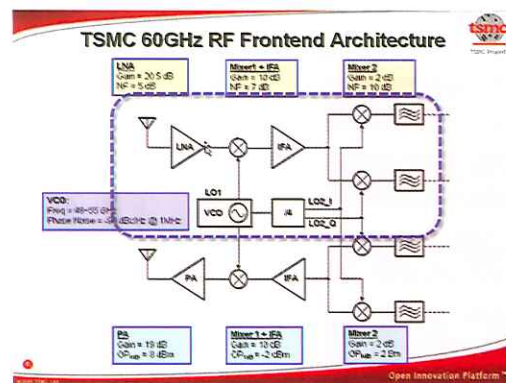
→ View full webinar at: <http://www.agilent.com/find/eesof-tsmc-60ghz-rdk>

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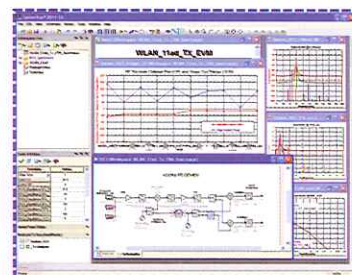
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Initial 60GHz Transceiver Architecture



- Initial architecture selection and block spec refinement with *SpectraSys*



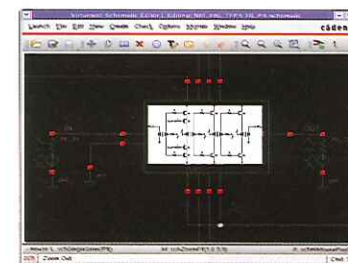
- Architecture and block spec validation vs. consistent 802.11ad TX/RX baseband references in *SystemVue*

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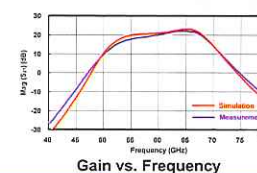
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TSMC 60-GHz CMOS mm-Wave RDK Power Amp Characterization in GoldenGate



Full characterization of performance metrics:
NF, Pout vs Pin, IP3, Load Pull, PAE, ACPR, ...



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What's New in RDK 4.0 – X-Parameter Generation

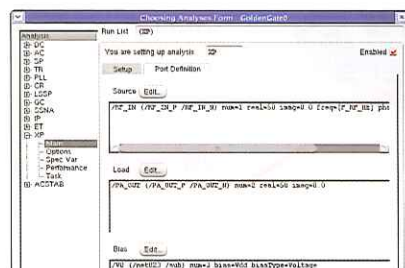
Full X-parameter generation

- New GoldenGate analysis type
 - XP
- Generated models exportable
 - ADS, SystemVue, GoldenGate



Full X-parameter simulation

- Using real models coming from measurements or simulations
- Tremendous speed-up by simulating a model rather than a full netlist



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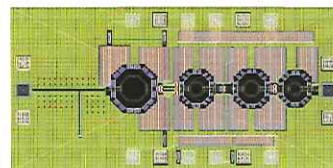
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TSMC 60-GHz CMOS mm-Wave RDK EM Verification with Momentum



Layout



EM simulation:

- Component level:** Input/output GSG pads, Transformers, Transmission lines
- Block level:** Passives + interconnects

Silicon-accurate nanometer RFIC process support:

- Automated layout pre-processing like via array merging
- Dummy metal fill and process scaling support
- Boolean layer operation for native MIM capacitor support

Cadence Virtuoso integration:

- Seamlessly integrated into the Cadence Virtuoso
- 3D Viewer with embedded visualization of surface currents or radiated fields provides insight on problem areas in layout
- Broad-band Spice Model generation for efficient use in time-domain simulations

Momentum officially qualified at TSMC:

- +50 Momentum Modules are available for TSMC processes down to 28 nm

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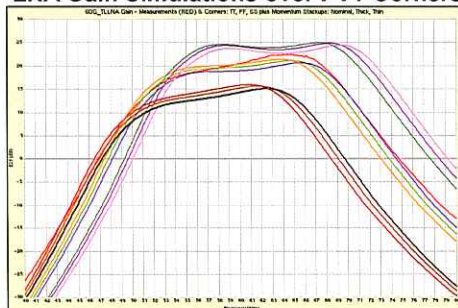
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What's New in RDK 4.0 – EM PVT Corner Analysis

- EM analysis performed with three stack-up files: Nominal, Thick and Thin
 - Circuit simulation performed at all combinations of EM corners and PDK corners TT, FF and SS
- Variations have impact of gain and frequency band
 - +/- 5 dB on gain
 - +/- 3 GHz band width

LNA Gain Simulations over PVT Corners



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Full Front-to-Back ADS PDK for TSMC's Dedicated "Integrated Passive Device" (IPD) Process



What is it?

- ADS PDK with Schematic, Layout, Substrate Definition file and DRC support for TSMC IPD 0.18um Process

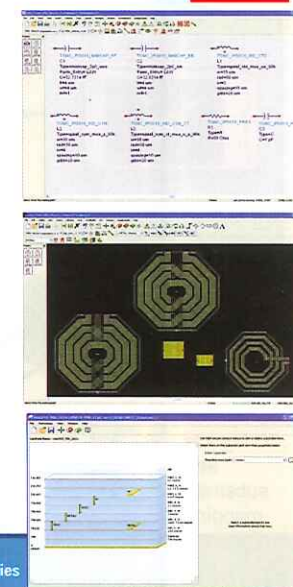
What does it include?

PDKs enable a complete ADS based flow and typically include the following features :

- Schematic entry
- Simulation
- Momentum EM solver stack-up files
- Layout including PCells
- DRC/LVS Check
- Microstrip lines
- MMIC/RFIC Toolbar for easy design

Design Elements:

- RF MIM Capacitors, Baseband MIM capacitors and RF Inductors



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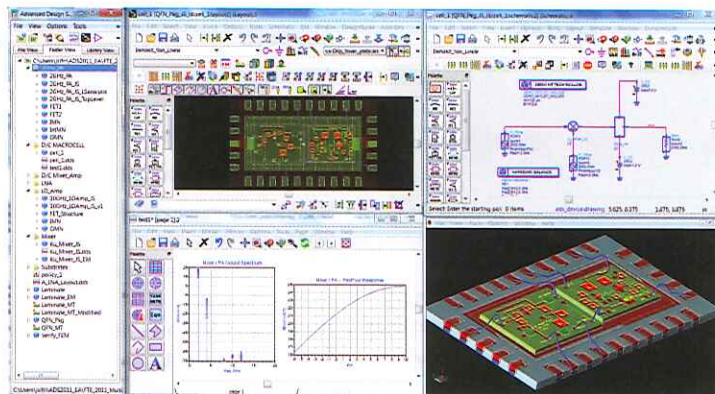
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ADS – Complete Front-to-back Design Platform for Small-scale RFICs & RF Modules

- Schematic Entry
- Simulators
 - System
 - Circuit
 - EM
- Data Display
- Layout
- DRC/LVS
- DFM support



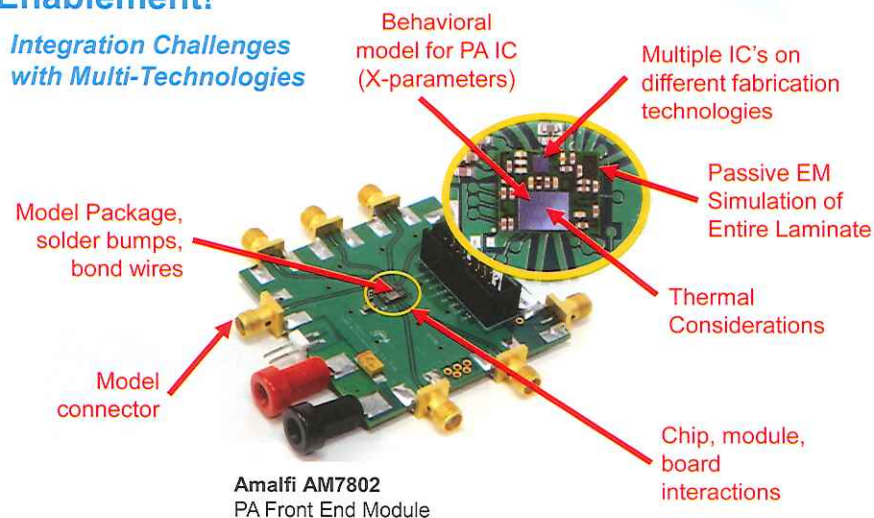
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What's next? Going Beyond IC Design Enablement!

Integration Challenges
with Multi-Technologies

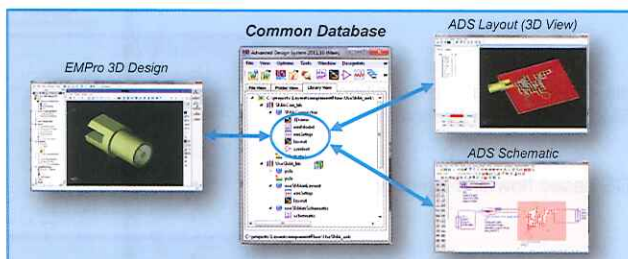


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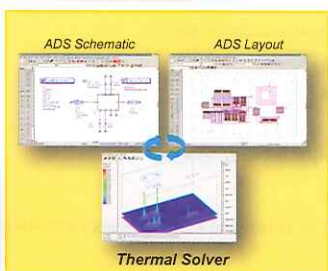
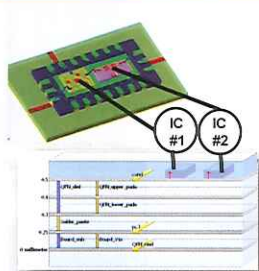
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Addressing the Multi-Technology Design Challenge



Chip-Module-Board design driving need for circuit simulation and 3DEM simulation share a common database and platform (no more files to transfer)

Module design requires core platform to handle side-by-side IC layouts and substrate mapping



Electro-Thermal Simulation required for 'thermally aware' circuit simulation that includes effects of on-chip temperature rise

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Summary



- Close foundry and EDA collaborations are key to ensure silicon-accurate results on RF process nodes
- We have seen two examples on how TSMC & Agilent Eesof support ual customers
- 60-GHz RDK – A silicon-proven MS/RF reference circuit and methodology packaged into a complete RF reference design kit (RDK)
- IPD design enablement – Hallo
- Collaboration extends beyond pure IC focus, since our customers design challenges go across design domains
 - Leveraging latest technologies from both sides!

More details at: <http://www.agilent.com/find/eesof-partners-tsmc>

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Silicon-Accurate Mixed-Signal Fractional-N PLL IP Design

Berkeley Design Automation & Silicon Creations

ABSTRACT

This presentation will describe the challenges in achieving silicon-accurate design and verification of a fractional-N PLL IP fabricated in the TSMC 28nm HP process. Silicon Creations supplies high-performance semi-custom analog and mixed-signal IP that can be optimized for each individual application. The designs include PLLs, DC-to-DC converters, data converters, high-speed I/O, and SerDes. Silicon Creations uses the Analog FastSPICE™ (AFS) Platform from Berkeley Design Automation for nanometer circuit verification. With the AFS Platform, designers increase their productivity and can perform large analog circuit signoff with nanometer SPICE accuracy. AFS is certified in TSMC SPICE-Qualification Program and AFS device noise sub-flow validated in TSMC AMS Reference Flow.

This paper provides details on the verification of programmable delta-sigma fractional-N PLL IP used as a multi-function, general purpose frequency synthesizer. The post-layout netlist of this circuit includes ~108 K elements with ~18.1 K MOS devices. The IP was fabricated using the TSMC 28nm HP process. AFS was used to characterize the VCO and to verify the closed-loop behavior of the post-layout PLL. For the VCO, the dominant noise source of the PLL, AFS Periodic Noise analysis was used to characterize the circuit over 12 temperature, frequency, and process corners, with excellent silicon correlation. For the postlayout closed-loop PLL verification, AFS demonstrated up to 18X speedup when compared with traditional SPICE for locking simulation and AFS Transient Noise results for PLL phase noise were within 1-2 dB of silicon measurement.



Silicon-Accurate Mixed-Signal Fractional-N PLL IP Design

Andrew Cole, Silicon Creations
David Lee, Berkeley Design Automation

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Introduction

- Presenting verification results of Fractional-N PLL IP
- Three way collaboration between:
 - Silicon Creations: 28nm precision analog IP development
 - TSMC: 28nm process with silicon accurate models
 - BDA: Device Noise Analysis in the Analog FastSPICE™ Platform



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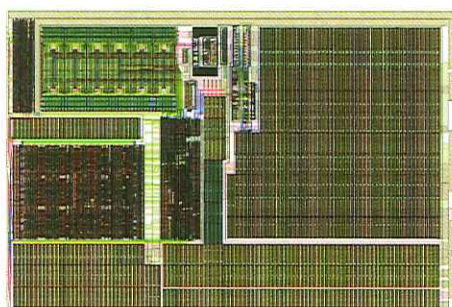
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IP That Works – First Time

- Product specifications grow ever more demanding
- Tradeoffs between performance, power, and area
- Customers expect to yield to specification on first silicon
- Stringent verification challenges



28nm PLL Layout

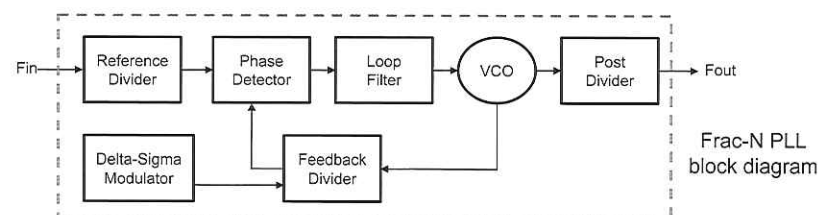
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Fractional-N PLL - Key Applications

- Clock signals for system logic
 - Provides flexibility of clock reference source and spread spectrum
 - High-speed logic needs low short term jitter, accurate for sufficient timing margin
 - Need to accurately predict random jitter from VCO → BDA's Analog FastSPICE™
 - Need to accurately predict supply-dependent deterministic jitter → BDA's Analog FastSPICE
- Timing for analog front ends and ADCs
 - Provides flexibility of frequency value and low jitter
 - Long term jitter determines distortion or noise floor - the key performance spec
 - AFS Transient Noise predicts random jitter from closed-loop PLL
 - Includes VCO noise, reference spurs and delta-sigma spurs



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Custom IP Verification Challenges

- Traditional SPICE simulators do not have performance and capacity
- Need nanometer SPICE accuracy to validate key specifications
- Need tighter tolerances to increase the dynamic range (>100dB)
- Need to include layout parasitics and device noise
- Long runs for verification and characterization

Fractional-N LC PLL		Specification
Critical Specs	Lock Range	1.6GHz to 3.2GHz
	Output Jitter	0.26ps RMS
	Phase noise @ 1MHz	-125dBc/Hz
	Reference spur	-71dBc
	Loop bandwidth	30kHz
	Power consumption	53mW @ 3.2GHz

- Accuracy
 - 60-120 dB dynamic range
 - Device noise bandwidth
- Long runs
 - PLL locking, jitter/phase noise
 - Integration w/ driven circuitry
- nm circuit characterization
 - Extracted parasitics: >200k
 - Device mismatch: >200 iters
 - PVT corners, process variation

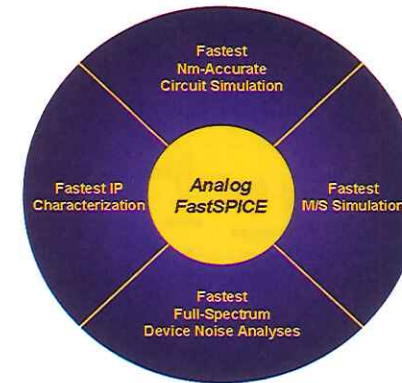
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The Verification Platform

Silicon Creations Selects Analog FastSPICE™ (AFS) Platform



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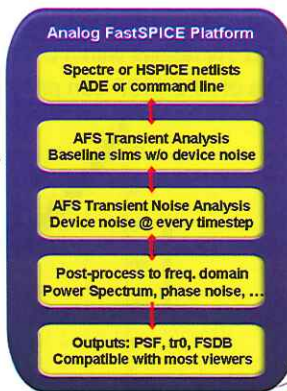
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AFS in TSMC AMS Reference Flow

Analog FastSPICE Transient Noise (AFS TN)

- **Functionality**
 - Random noise for each source at each timestep
 - White & flicker noise sources
 - Noise based on instantaneous device bias
 - Turn noise on/off at block level
- **Accuracy**
 - Solve stochastic equations for noisy waveforms
 - Advanced timestep control for random noise
 - Improved tolerance settings for transient noise
 - Ensures statistical accuracy for device noise
 - Accurate post-processing method
- **Performance and capacity**
 - AFS Transient is 5x-10x faster vs. traditional SPICE (1-core)
 - AFS TN vs. AFS Transient <2x per timestep
 - AFS TN supports AFS Multi-Core Parallel mode
 - Over 10M element capacity



TSMC Analog Mixed-Signal Reference Flow 2.0

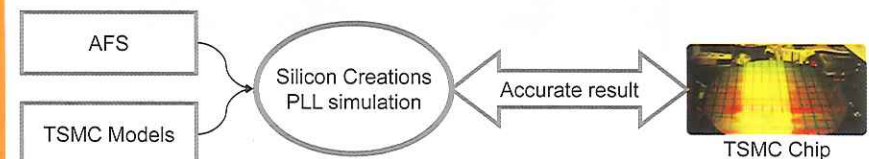
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Simulator and 28nm Model Accuracy

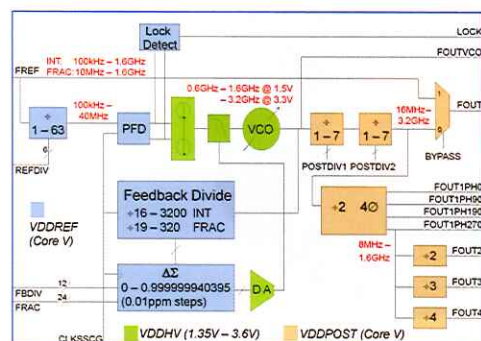
- The accuracy of the result of a simulation of a circuit is a function of
 - Simulator accuracy
 - Device model accuracy
- Simulator:
 - AFS delivers nanometer SPICE accuracy
 - AFS Noise and Jitter analysis based on BDA developed theory
 - Based on advanced stochastic nonlinear theory
 - Recognized as most accurate theory in industry today
- Device Models:
 - New first-order effects due to device noise require more accurate model parameter extraction
 - Device noise model parameters used in simulation from TSMC 28nm PDK



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Programmable Delta-Sigma Fractional-N PLL

- Multi-function, general purpose frequency synthesizer
- Best-in-class jitter performance, low power, and small area footprint.
- Multiple clocking applications and spread-spectrum clock generation
- Feed-forward jitter compensation for low jitter



- Input frequency range 100kHz - 1.6GHz
- Output frequency range 2MHz - 3.2GHz
- LT jitter <5ps RMS in fractional mode
- 24-bit fractional accuracy
- 4:1 VCO frequency range
- ~108K elements with ~18.1 KMOS

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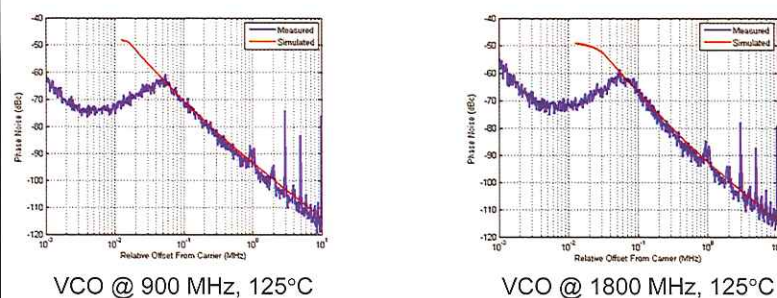
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VCO Characterization

- VCO is the dominant source of phase noise for the PLL
- Phase noise was characterized across freq., process, and temp.
- AFS full-spectrum vconoise versus measurements on the full PLL
- A total of 12 corners with excellent silicon correlation
- Impulse Sensitivity Function (ISF) and noise contribution for all devices

VCO vs. Measured Frac-N PLL - Process Corner TT



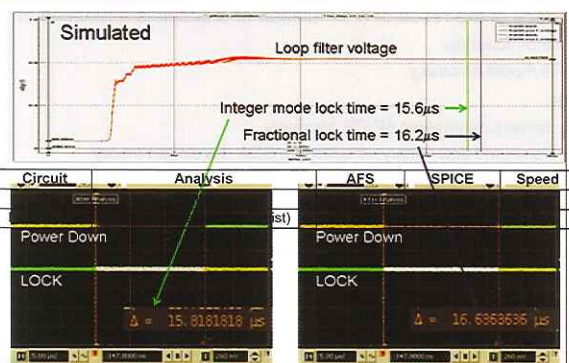
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PLL Post-Layout Locking Simulation



Circuit	Analysis	AFS	SPICE	Speed
VCO	Transient	1.5 min	14 min	9.3×
Frac-N PLL	Transient (extracted netlist)	~30 hr	~3 wk	~18×

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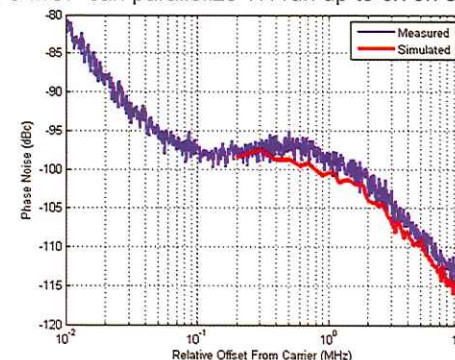
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PLL Closed-Loop Transient Noise Simulation

- AFS Transient Noise (TN) analysis verified the PLL phase noise
- Includes the full-spectrum effects of device noise
- Handled the complete post-layout PLL with nanometer SPICE accuracy
- AFS TN results within 0-3 dB of silicon measurement
- Use of AFS MCP can parallelize TN run up to 8x on single machine



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Conclusion

- The AFS Platform from Berkeley Design Automation has
 - Improved analog and mixed-signal circuit design signoff flow
 - Increased design productivity and reduced risk
- For the Frac-N PLL closed-loop post-layout verification
 - Need transient noise to validate phase noise and spurs
 - AFS TN results within 0-3 dB of silicon measurement
 - AFS demonstrated up to 18x speedup in locking simulation
- Silicon Creations can now
 - Perform SPICE-level signoff of large analog circuits
 - Accurately predict PLL phase noise and high-speed I/O jitter

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Chip-Partitioning Trends in Systems Using Ultra Deep-Submicron SoCs

Cosmic Circuits

ABSTRACT

The integration of analog functionality on a digital chip becomes an intense debate during the chip architecture phase for emerging analog-intensive products and gets re-ignited every time an advanced technology node becomes mature. While integration offers the advantages of power and foot-print, few companies have been able to create a complete system on a single chip. A cell-phone system will include components as diverse as a processor, digital baseband and networking subsystems, the analog baseband subsystem, high-speed connectivity subsystems, power-management unit and the RF subsystem making integration a tall order. The more judicious solution to take is a hybrid approach where the system is partitioned between two silicon dies – an SoC die in an ultra-deep-submicron technology such as 28nm and an analog die in a analog CMOS technology such as 0.18 μ m. Every block in the system is then analyzed to determine whether it needs to be developed in the UDSM process or an analog CMOS technology to achieve overall system optimization on the key parameters such as foot-print, cost, power, time-to-market and development cost. In this presentation, we consider several analog, mixed-signal blocks/subsystems and based on our experience working with these subsystems across multiple technology nodes, share our outlook on the partition trends considering a chipset that includes a 28nm SoC and a 0.18 μ m analog die.



ANALOG, MIXED-SIGNAL & RF

Chip-partitioning Trends in Systems using Ultra deep-submicron SoCs

Sundararajan Krishnan (PK)
Director, IP




— Differentiated Analog IP —

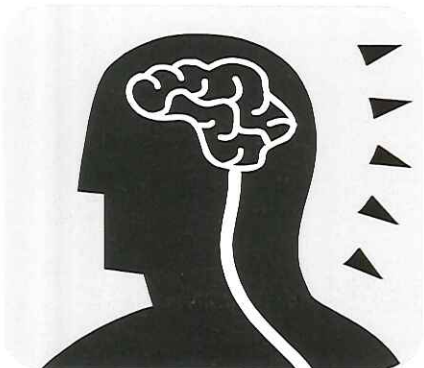

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Overview

- Introduction
- Design philosophies for ultra deep sub-micron technologies
- Scaling benefits for mixed-signal circuits
- Ultra deep sub-micron and high-voltage circuits?
- Conclusions


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The Integration Conundrum




Cost

Time-to-market

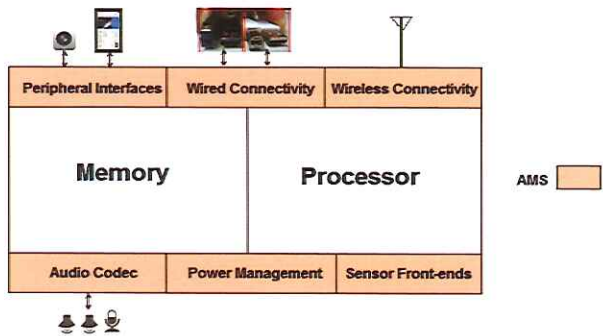
Power

Development cost


Foot-print


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The Analog/mixed-signal Pieces of the Puzzle



- Peripheral voltage/power requirements dictated by legacy/user rather than technology scaling
 - Newer/emerging connectivity standards in tune with technology-scaling driven voltage requirements
- Internal blocks can exploit advantages offered by technology


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The Partitioning Options

- Conventional partitioning
 - Digital engine in the SoC
 - AMS circuits in the companion chip
- Integration
 - Single SoC that integrates all functions
- Hybrid
 - Multi-die solution with single package

The integration-decision matrix

	Must integrate?	High-voltage?	Specialty IO?	Will area, power scale?	Risk of migration
Wired Connectivity	Yes	Yes	Yes	Likely	Doesn't matter
Wireless Connectivity	No	No	No	Likely	High (if RF is included); Low (excluding RF)
Peripheral Interfaces	No	No	No	Likely	Low
Audio Codec	No	Yes	Yes	Scaling for converters; amplifiers don't scale	High (if driver amplifiers are included); low (excluding driver amplifiers)
High-current power management	No	Yes	Yes	Unlikely	High

The AMS-designer View of Technology Scaling



Speed



Reduced supply voltage

Lower Parasitic

Leakage

Digital-gate density

Layout effects

Design Challenges in UDSM Nodes

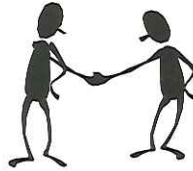
- Analog area increases in 28nm
 - Passive area (capacitors) increases due to RDR
 - Transistor area impacted by max. width considerations, WPE
- Design complexity
 - 5V/3.3V legacy support for interfaces using 1.8V transistors
 - Increased reliability checks, custom ESDs
- Simulation complexity
 - Montecarlo with local/global variations vs. traditional corner sims (too pessimistic)
 - Layout-aware simulations (LPE, etc.) → increased simulation time
 - Usage of multi-Vt devices for power optimization increases corner-matrix

Overcoming Design Challenges

AMS designers become "system" engineers with a digital-CMOS outlook to analog design

Digital

Signal processing
Computing/Error Control
Coarse loop-control



What was

Analog

Interface/Bias circuits
Simplified amplifiers
Fine loop-control

Analog/digital **system** partition in 0.13um

is now

Analog/digital **block** partition in 28nm



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High-speed SERDES: 65nm vs 28nm

Process Features

Logic Speed

Lower parasitic



Impact on Design

Synthesizable
high-speed digital

Timing-critical blocks
easier to design

Smaller current transients → simpler
power-supply generation



Results for M-PHY

Area and power reduce by 40% from
65nm to 28nm



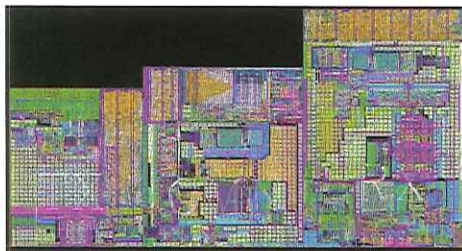
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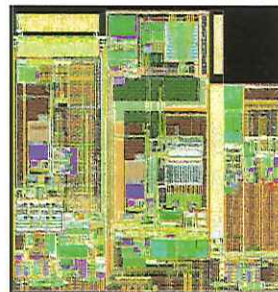
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High-speed SERDES: 65nm vs 28nm

TSMC65LP



TSMC28HPM



40% reduction in area in 28nm despite no scaling in the
conventional analog blocks!



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Design Philosophy for Advanced Nodes - ADCs

Process Features

Device Speed

Digital Density



Impact on Design

Digital-friendly architectures

High-speed SAR/Σ-Δ
ADCs

Digital calibration for
pipeline ADCs



Results for a 10b high-speed ADC

2X scaling in power from 65nm to 28nm



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PLLs: 65nm vs 28nm

Process Features

Logic Speed

Lower parasitic



Impact on Design

Synthesizable high-speed digital

Timing-critical blocks easier to design

Digital PLL architectures → single supply operation → lower power



Results for Freq. Synthesis PLL

2X scaling in power from 65nm to 28nm

Power-Management and Audio Amplifiers

- 5V support a minimum for most systems
- Supporting 5V with 1.8V transistors is complex
 - Inefficient power-generation
 - Cascoded structures → larger I²R losses
 - Complex keep-alive circuits (reliability) → larger standby currents
 - Larger area
 - Increased cost
 - High-voltage specialty IO
 - Larger pad count (supply generation, distribution)
- Similar arguments hold for high-power audio amplifiers (1-2W speaker drivers)
- Intelligent power-management option presented by an integrated solution can be easily achieved with a custom ASIC using a well-defined die-to-die interface

Chip-partitioning Summary

	Pros	Cons	
Conventional – digital engine in the SoC, AMS circuits in the companion chip	Ease of design, development cost, TTM	Package foot-print, higher power (AMS designs don't utilize the advantages offered by technology scaling)	
Integration – single SoC that integrates all functions	Package foot-print, minimum interfaces (reduced interface power)	Development cost, standby power (reliability circuits), inefficient power generation	
Hybrid approach – multi-die solution with single package	Marries benefits of conventional and hybrid approach. Potential for cost-savings	System-design complexity increases	

Conclusions

- Hybrid-approach (multi-die solution with single package) is the best approach to optimize the system solution
- Mixed-signal circuits scale with technology and will continue to do so. These offer a clear case for integration with the digital SoC
 - Design techniques will evolve to take advantage of the digital speed and density
- Power circuits and Audio front-ends are constrained by system-imposed voltage/power requirements.
 - Will be designed in a mature technology with a well-defined control interface
- Sensor front-end circuits will be integrated in the mature technology die for cost reasons



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**CMOS Silicon Millimeterwave Design Closure on
Integrated Fullwave Electromagnetic Simulation and
Extraction Platform with a Real Silicon Design Case**
Lorentz & Stanford University



ABSTRACT

CMOS silicon millimeterwave designs are made possible by the advancement of process device f_t and necessary by the vast potential applications in consumer electronics, communications, imaging, and radar detections. Compared to regular RF designs, the critical design challenges for a real silicon millimeterwave design closure solution are shifted from circuit design with signal integrity concerns to heavy electromagnetic and circuit co-designs. In this presentation, we illustrate such a design shift with real case study. We further present an integrated fullwave electromagnetic simulation/extraction platform that is being effectively used to design and optimize electromagnetic devices such as inductors and transmission lines with EM/circuit co-simulation. More importantly, this platform provides fullwave electromagnetic extractions for critical net and transmission lines as part of the LVS/LPE-based extraction flow. Nets that carry DC/low-frequency power or signals are extracted with traditional RC extraction tools. Nets that carry high-frequencies (up to Terahertz) are extracted with the fullwave EM accuracy with models automatically backannotated to the circuit netlist.

We present a real Stanford University silicon design case based on this integrated fullwave EM platform and compare this with the traditional manual EM modeling and stitching method. We show that not only we can precisely predict the silicon results with this sign-off capability, but also dramatically increase design productivity for silicon millimeterwave designs.



CMOS silicon millimeterwave design closure on integrated fullwave electromagnetic simulation and extraction platform with a real silicon design case

Jinsong Zhao

Lorentz Solution, Inc

Kamal Aggarwal, Ada Poon

Stanford University

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SOLUTION**

**STANFORD
UNIVERSITY**

Seminar Outline

- ❖ **Challenges for silicon millimeter-wave designs**
- ❖ **EM Design Platform**
 - Device-level designs and verification
 - Circuit-level EM signal integrity flow
- ❖ **A Real Silicon Millimeter designs**

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Millimeterwave

- ❖ **What is millimeterwave?**
 - Extremely high frequency (EHF) runs the range 30GHz-300GHz, has a wavelength of ten to one millimeter, and thus is also called millimeter wave (mmW).
- ❖ **CMOS silicon design in mmW**
 - Narrow-band design mmW to utilize the allocated bandwidths
 - ISM band (59-64GHz)/Unlicensed
 - Fixed Point-to-Point Services (77GHz)
 - Vehicular Radar (24GHz)
 - Broadband design in transceivers
 - Frequency-domain models accuracy > 100Ghz

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Design Challenges for RFIC/HS Analog Designs

- ❖ **RFIC/HS analog designs are device-centric**
- ❖ **Challenges in RFIC/HS analog design**
 - Active devices dominant for circuit performance
 - Passive devices key for frequency selection and phase/jitter performance
 - Interconnects with parasitic extraction as a second-order signal integrity sign-off
 - EM/substrate isolation sometimes causes issue that needs more robust methodology

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SOLUTION**

Design Challenges for MM-wave Designs

❖ MM-wave designs are EM-centric

❖ Challenges in MM-wave design

- EM structure design effects more dominant and elusive
- Lumped circuit design method shift to distributed transmission-line circuit designs, but without proper ground plane to localize EM effects
- Passive devices are smaller, need more protective structure, and hard "silicon verify."
- Interconnects no longer second order effects; they should be verified at device-level accuracy.
- EM/substrate isolation must be rigorously modeled and designed.

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EM Design Platform

❖ IC designs are done within two platforms

- Foundry PDK platform: Devices, Rules for sign-off (DRC, LVS, PEX)
- Custom IC EDA platform: Schematic/simulation/layout, DRC/LVS/PEX

❖ RF and high-speed analog designs are underserved by these two platforms

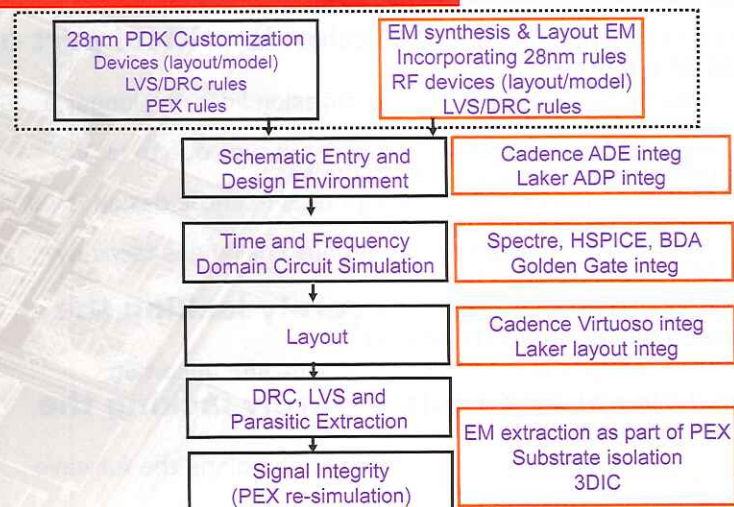
- Foundry PDK lacks the critical RF passive devices, and most fabless companies resort to expert support, who must understand EM, modeling, process, and CAD integration
- No EM sign-off the same way parasitic extraction
- Signal integrity tools severely lagging. There needs to too much debugging.

❖ EM Design Platform is the best approach for RF and mmW designs

- EM design must be part of RF/mmW design flow; no longer a standalone effort
- EM design must be a team effort with shared database, shared design philosophy and reproducible results
- EM design must have the most rigorous EM accuracy to predict the silicon results
- EM design must provide maximum design automation to achieve team productivity and true first-pass silicon

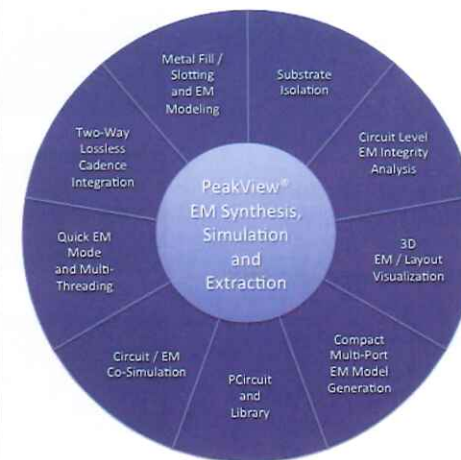
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Design Flow with EM Design Platform



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Major Technical Capabilities

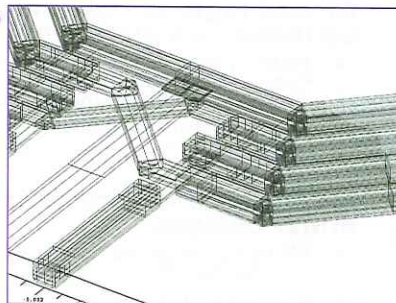


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EM Accuracy and Silicon Correlation

❖ How to achieve MMW EM accuracy?

- Must be fullwave
- Must be 3D planar/true 3D
- Must be structural
- Maximum physics care
 - EM theory
 - Circuit theory
 - Total consistency
- Maximum numerical care
 - Convergence test
 - Dynamic range test
- Reasonable performance

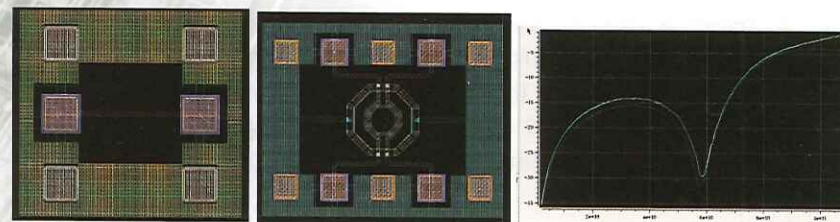


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Silicon Correlation

❖ Is it possible to do silicon correlation at MMW?

- Possible, but it requires real understanding of limits of process variation, measurement, calibration/de-embedding, and EM results
- Many traditional RF methods are no longer valid



Layout/Silicon results courtesy of TSMC

S11 of transmission line up to 110GHz

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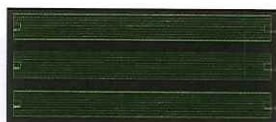
Transmission Line Synthesis for MMW

❖ A rich set of transmission line designs for MMW EM synthesis, including

- Micro-strip line
- Differential line
- CPW
- Solid/slot shielding structures
- Grounded/floating shielding structures
- Extremely flexible layer selection
- User extensible

❖ Physics-based models

- Physics-based models are also developed for reliable transient simulations.



CPW



CPW with solid shield



CPW with floating slot shield

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Maximum EM Design Automation: Interconnect EM Extraction

❖ Interconnect EM extraction is critical part of MMW design

- Interconnect behaves like transmission lines, no longer a second-order effects
- Worse, interconnects have coupling issues due to lack of proper ground and complex routings
- Shift from device-centric design to EM-centric design is full of learning lessons
- MMW design dramatizes the serious challenges faced by RF/HS analog designs

❖ Traditional EM tools severely lacking the "maximum automation"

- MMW designs are thus very laborious and uncertain

❖ Traditional PEX tools severely lacking the "EM accuracy"

- Inductance itself was not done well, let alone the fullwave effects and structural details

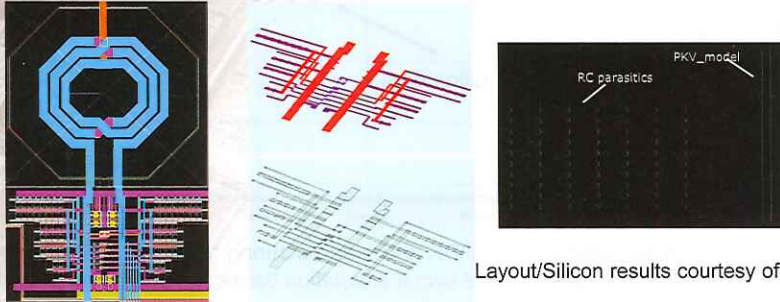
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Interconnect EM Analysis

❖ Peakview High Frequency Designer (HFD)

- Complement the layout parasitic extraction tool by EM modeling certain critical nets
- Automate the flow of full-wave EM model generation and back-annotation for interconnect analysis

❖ Does it work? How to mitigate the potential risk?



Layout/Silicon results courtesy of TSMC

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SOLUTION**

Real Design with EM Design Platform

❖ Distributed Phase Shifter

- Frequency Range : 50 – 70 GHz
- Multiple Phase settings

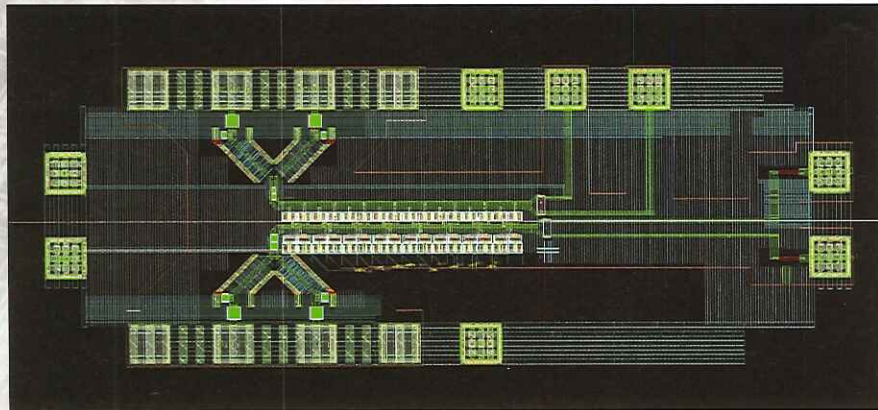
❖ EM challenges

- No "Calibre" equivalent at mm-wave to model
 - Differential transmission line
 - CPW lines
 - Interconnects
- Piece-by-piece modeling only available solution
 - Time consuming
 - Doesn't represent true design parasitics

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MMW Layout

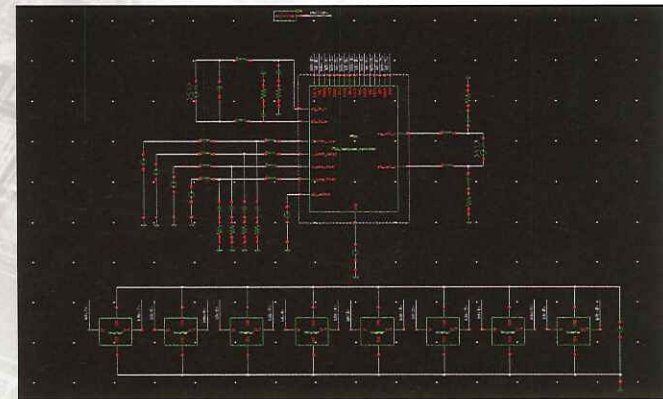
Includes synthesized EM device



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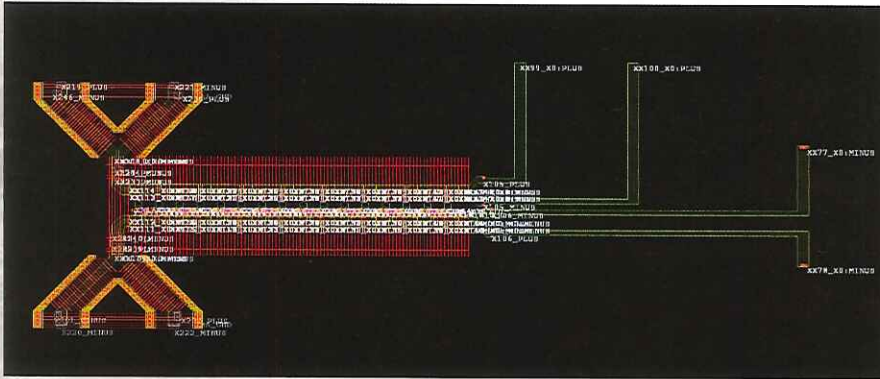
Test Bench

Circuit/EM combined into final test bench



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Extracted Layout by HFD

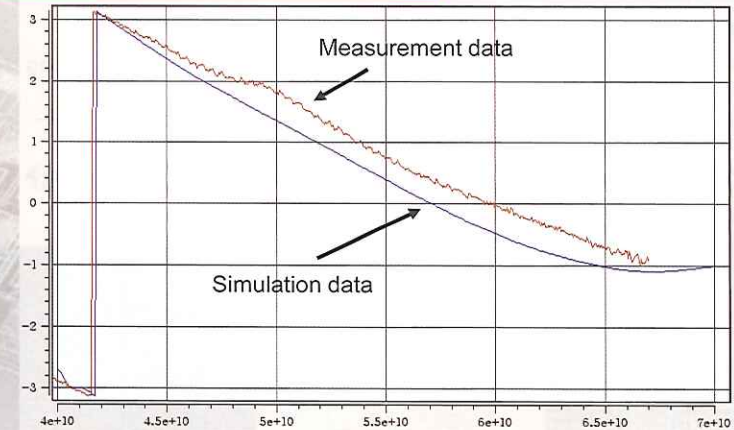


Total ports extracted: 256.

Acknowledgement: layout extracted using Calibre LVS and xRC from Mentor Graphics

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SOLUTION**

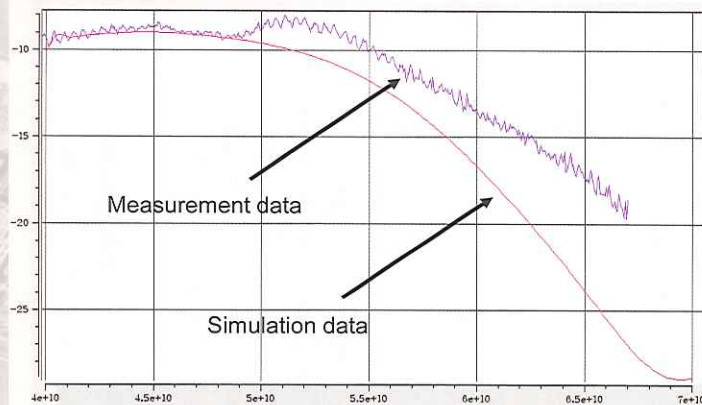
Comparison: Phase



Acknowledgement: PDK and manufacturing provided by TSMC
Design and circuit simulation based on Cadence tools

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SOLUTION**

Comparison: Magnitude



Acknowledgement: PDK and manufacturing provided by TSMC
Design and circuit simulation based on Cadence tools

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SOLUTION**

Conclusion

- ❖ **EM Design platform as part of PDK for MMW designs**
 - Enables the PDK to be RF and MMW design ready
 - Enables the paradigm shift from device-centric design to EM-centric design
 - Reins in the uncertainty encountered in MMW designs, especially uncertainty related to interconnect and EM couplings.
- ❖ **A strong collaboration among industry/university, foundry and EDA companies made this project possible.**

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SOLUTION**

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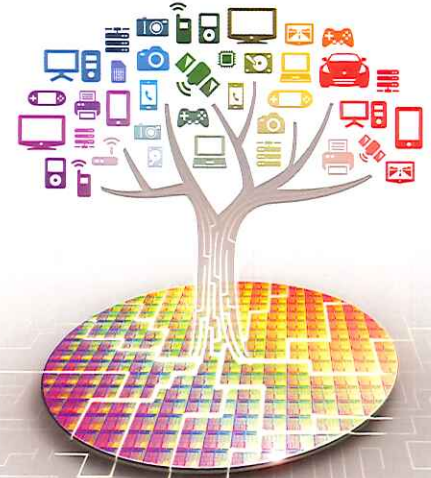
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Print-Only Papers

TSMC 2012 Open Innovation Platform® Ecosystem Forum

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10GHz to 100GHz CMOS Passives Design; the Challenges and Some Solutions

Integrand Software



ABSTRACT

With the introduction of high-performance and nano-scale CMOS technologies, silicon has made its foray into very high speed and millimeter wave applications. SerDes blocks that used in high-speed networks routinely operate in the 10GHz to 60GHz range. Wireless data links including chip-to-chip and base-station to base-station have standards in the 60GHz band. Si-based receivers and transmitters are being developed for automotive radar, atmosphere monitoring and medical applications in the 60GHz to 100GHz range.

There are a number of challenges in the design and modeling of circuits at these frequencies involving both active and passives. In this paper we discuss some of the challenges and solutions for the modeling of passives at these high frequencies. As frequencies increase, the coupling between on chip passives becomes critical. For example isolation between different inductors on a chip becomes very important. In addition, stray interconnect lines surrounding sensitive passives can resonate once they become a fraction of a wave length. Dummy and metal fill can introduce significant loss in the system. Radiation effects and time-of-flight now matter as passives can start to radiate and even become mini-antennas at very high frequencies. The Q of structures like MOM capacitors become the bottleneck for high frequency applications (instead of inductors). More importantly, the passive circuits themselves change from “lumped-passives” like inductors and capacitors to distributed $\frac{1}{4}$ wavelength passive structures. Passive components that were traditionally found on boards for microwave circuits are now being implemented in silicon. Instead of using inductors and transformers we are starting to see the introduction of passive couplers and power splitters and combiners like Wilkinson Dividers, 6dB Couplers, Quadrature hybrids.

It is well known that Maxwell’s equations can fully describe the physics of these problems. The difficulty lies in adapting the current generation of Electro Magnetic (EM) tools to accurately and efficiently solve the problems. Quasi-static approximations simply do not suffice. Meshing of structures being simulated needs to be fine enough to capture the very small skin depth at these frequencies. The challenge lies in the implementation of the 3D full-wave Electro Magnetic (EM) solvers which can correctly model the effects accurately and efficiently. In this paper, we describe the use of the EMX 3D simulator to model these high frequency effects. We describe how the fast multipole method (FMM) algorithm can be very efficient for even solving the problems arising from the large problems and dense meshing that arise from the solution at high frequencies. We also describe a method for automatically modeling pattern-dependent effects within the EMX 3D simulator. EMX’s process file format allows the specification of width and spacing dependencies. We show that EMX can model MoM capacitors and stacked inductors whose behavior is sensitive to pattern dependencies. In addition, we have a number of novel circuits and implementations by our mutual customers, using a variety of TSMC technologies (from 130nm to 28nm), that validate the use of EMX at very high frequencies.





10GHz to 100GHz CMOS passives design; the challenges and some solutions.

Dr. Sharad Kapur

Integrand Software, Inc.
EMX

TSMC Open Innovation Platform® Ecosystem Forum, October 2012



Outline

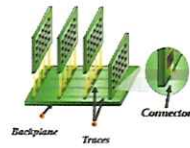
- Applications at 10GHz-100GHz
- Modeling of passives at high frequencies
- 3D EM simulation of IC structures
 - Methods for accurate and efficient solution
- Design issues at high frequencies
- High frequency passives
 - Couplers, dividers, quadrature-hybrids
- Novel IC examples from industry and academia
 - Validation and comparison to measurements
 - 60GHz to 200GHz
- Challenges ahead
- Conclusion

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Applications at 10-100 GHz and above

- SerDes
 - 10GHz-40GHz
- Wireless links (60G)
 - Chip-to-Chip, base station-to-base station, Wireless HDTV
- FMCW imaging (60G)
 - Collision avoidance radar (77G)
 - D-band (100G to 170G)
 - E-band, W-band: (70G-100G)
- Medical applications: 200G+
 - Wireless detection of vital signs

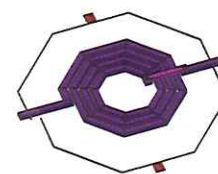


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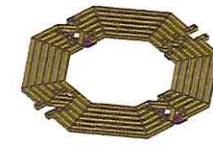
Passive structures



Inductor



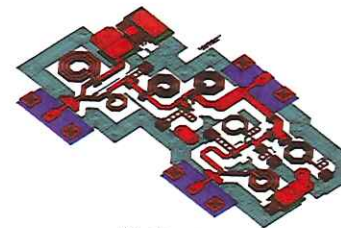
Shielding



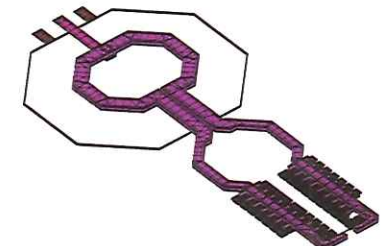
Transformer



MOM capacitor



Diplexer



VCO with capacitor bank

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Challenges at high frequencies

- Modeling of active devices
 - Depends a lot on the type of technology, SiGe, BiCMOS, CMOS, GaAs
- Modeling of passive components
 - Largely dependent on the metallization and substrate
 - Does not matter if it is CMOS, SiGe or GaAs
- This talk will be about modeling of passive structures and components at very high frequencies

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The physics

Behavior of passives described "fully" by Maxwell's equations

Differential Form

$$\begin{aligned}\nabla \cdot \mathbf{E} &= \frac{\rho}{\epsilon_0} \\ \nabla \cdot \mathbf{B} &= 0 \\ \nabla \times \mathbf{E} &= -\frac{\partial \mathbf{B}}{\partial t} \\ \nabla \times \mathbf{B} &= \mu_0 \mathbf{J} + \mu_0 \epsilon_0 \frac{\partial \mathbf{E}}{\partial t}\end{aligned}$$

Integral Form

$$\begin{aligned}E_s(r) &= \frac{1}{\sigma} J(r) + j\omega A(r) + \nabla \phi(r) \\ A(r) &= \int G_A(r, r') J(r') dr' \\ \phi(r) &= \int G_\phi(r, r') \rho(r') dr'\end{aligned}$$

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Differential vs. Integral

Differential formulations

- Finite-element, FDTD
- Flexible
- Imposes no constraint on shape of metals, dielectric regions
- Need to enforce Maxwell's equations everywhere surrounding the object
- Leads to large sparse matrix solve

Integral formulations

- MoM, BEM, Integral formulations
- Planar dielectrics, conductors
- Need to enforce Maxwell's equations only on conductors (Green's theorem)
- Leads to smaller dense matrix to solve
- Many techniques developed recently
- For IC passives this approach is the best

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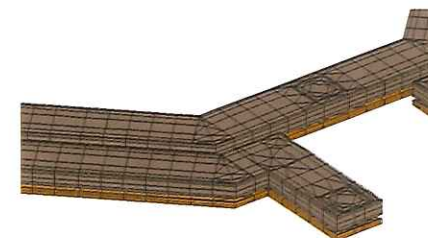
7

3D planar EM simulation

- **EMX®** is a 3D EM simulator
- 3D volume integral formulation (time-harmonic)
- Unknowns are charges and currents
 - Surface charges and volume currents
- Includes retardation (time of flight)
- Also skin effect is critical at higher frequencies so you need a volume current and meshing of the metals

$$\begin{aligned}A(r) &= \int G_A(r, r') J(r') dr' \\ \phi(r) &= \int G_\phi(r, r') \rho(r') dr'\end{aligned}$$

$$E_s(r) = \frac{1}{\sigma} J(r) + j\omega A(r) + \nabla \phi(r)$$



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Matrix formulation

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$$E_s(r) = \frac{1}{\sigma} J(r) + j\omega A(r) + \nabla\phi(r) \quad (\text{continuous form})$$



$$Ax = B \quad (A \text{ is a dense matrix})$$

- Suppose that N elements in the mesh
- Conventional approach $O(N^3)$ time and $O(N^2)$ memory
 - Cost is prohibitive
 - Double the size of the problem 8X time

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Innovations in numerics (GMRES+FMM)

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$$Ax = b$$

- Iterative methods (GMRES, Yale, 1986)
- Matrix vector products instead of matrix inversion
 - $K_n = \{b, Ab, A^2b, \dots, A^n b\}$
- This reduced the time to $O(N^2)$
- The Fast Multipole Method was developed in 1987
- Applied to capacitance/EM solution
 - FastCap, Fast Henry, (1990s). (MIT/White)
 - IES³, Bell Labs, Kapur and Long, (1990s)
- Used in EMX $O(N)$
- These sorts of problems can be solved in **linear time**

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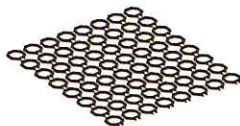
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Time and memory scaling

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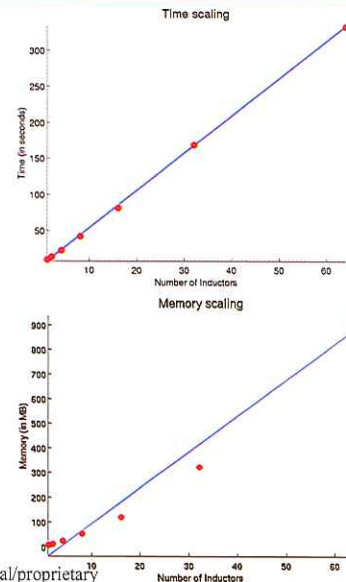


1 inductor



64 inductors

- Single frequency simulation (including iterative solve)
- Compare speed and memory for 1, 2, 4, 8, ..., 64 inductors
- Very important that it is a linear time solution



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Tech trends

- Thick metals
 - 0.1um to 8um copper
- High-resistivity substrates
 - 10 Ω -cm to 1000 Ω -cm
- Fine feature sizes
 - 0.05 μ m width at 28nm
- Many metal layers
 - High density capacitors
- Easier for MOM/Integral solutions that do not need to discretize dielectric interfaces and only conductors

	h=0.0, $\epsilon=1$
	h=0.25 μ m, $\epsilon=2$
	h=0.075 μ m, $\epsilon=7.8$
metal9	h=3 μ m, $\epsilon=4$
via8	h=0.11 μ m, $\epsilon=7.8$
	h=0.725 μ m, $\epsilon=4$
	h=0.075 μ m, $\epsilon=7.8$
metal8	h=0.775 μ m, $\epsilon=4$
via7cm	h=0.05 μ m, $\epsilon=7.8$
clm	
via7	h=0.62 μ m, $\epsilon=4$
via7cbm	
clm	
metal7	h=0.05 μ m, $\epsilon=5$
via6	h=0.1 μ m, $\epsilon=2$
metal6	h=0.05 μ m, $\epsilon=4$
metal5	h=0.05 μ m, $\epsilon=5$
via5	h=0.1 μ m, $\epsilon=2$
metal4	h=0.05 μ m, $\epsilon=4$
via4	h=0.05 μ m, $\epsilon=2$
metal3	h=0.05 μ m, $\epsilon=4$
via3	h=0.1 μ m, $\epsilon=2$
metal2	h=0.05 μ m, $\epsilon=4$
via2	h=0.1 μ m, $\epsilon=2$
metal1	h=0.05 μ m, $\epsilon=4$
via1	h=0.1 μ m, $\epsilon=2$
metal0	h=0.05 μ m, $\epsilon=4$
via0	h=0.1 μ m, $\epsilon=2$
metal1	h=0.05 μ m, $\epsilon=4$
metal1	h=0.1 μ m, $\epsilon=2$
diffcont	h=0.31 μ m, $\epsilon=4$
diff	h=0.3 μ m, $\epsilon=3.9$

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TSMC iRCX technology files

- Accurate process parameters are critical for EM simulation
- TSMC iRCX file provides a detailed process information
 - Metal, dielectric properties
 - Temperature dependence
 - Statistics and corner cases
 - Width-spacing dependent properties
 - Designer does not have to enter information from design manual
 - Removes sources of error
- Width and spacing properties (paper at RFIC 09 with TSMC)
 - Mimics fabrication process
 - shows that this significantly improves simulation accuracy for passive components like inductors and MOM capacitors.

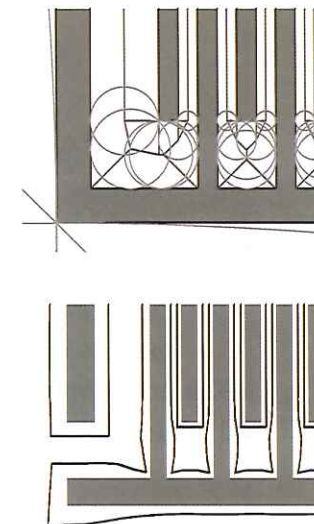
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Mimicking the TSMC fabrication in EMX

- EMX uses Voronoi diagrams to capture the width-and-spacing dependent parameters in the iRCX files
- These Voronoi diagrams are used to alter the drawn layout to mimic the fabrication process
- The shaded region shows the "drawn" layout and the "line" shows the modified layout according to the iRCX rules



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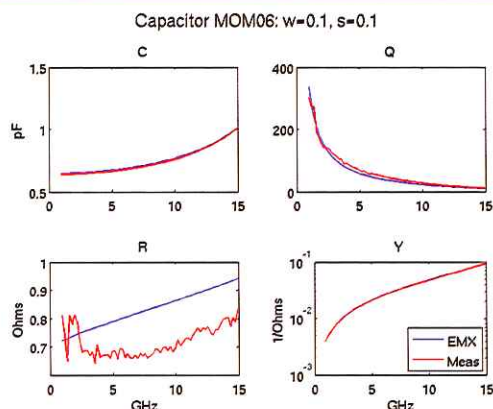
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MOM (finger)capacitor



3D mesh of 0.6pF Cap



Example	Ports	Freq Range	Size	1 CPU		8 CPUs	
				Mem.	Time	Mem.	Time
MoM capacitor	2	0.2GHz-20GHz	48,997	1140MB	19m12s	2591MB	5m59s

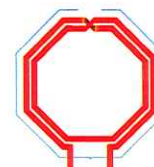
Courtesy: TSMC. 65nm RFCMOS, 9LM thick metal technology. Published at RFIC 2009
 "Including Pattern-Dependent Effects in Electromagnetic Simulations of On-Chip Passive Components", Integrand and TSMC
 Not confidential/proprietary

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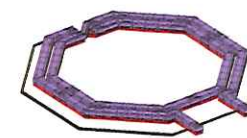
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Issues at high frequencies

- At high frequencies the skin effect is a significant issue
- Meshes need to be finer to incorporate these effects
- This leads to larger problem size (smaller structures?)



1GHz



1um mesh



60GHz



0.1um mesh

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Full-wave vs. quasi-static

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$$\phi(r) = \int G_{\phi}(r, r') \rho(r') dr'$$

$$G^{\phi}(\mathbf{r}, \mathbf{r}') = \frac{1}{4\pi\epsilon_0} \frac{e^{-j\omega|\mathbf{r}-\mathbf{r}'|/c}}{|\mathbf{r}-\mathbf{r}'|},$$

- Time of flight becomes important once frequency is "large" compared to the speed of light
 - Electrical length of structure is important
 - Specially important for electrically long structures
- Cannot compromise on using a quasi-static solution
- Laplace regime...not yet Helmholtz.

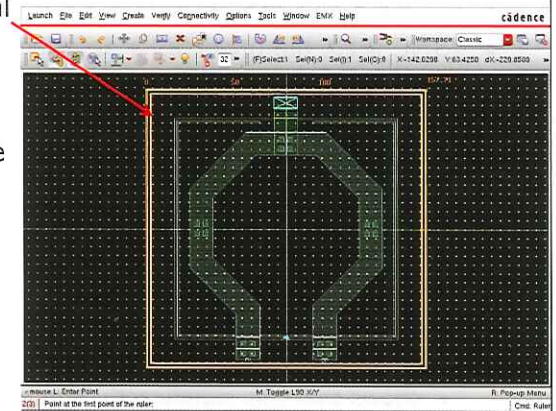
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Guard rings

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- Use of guard rings or seal rings in layout
- The ring is a loop of metal
- May be a metal line close to the inductor (supply line or bias line)



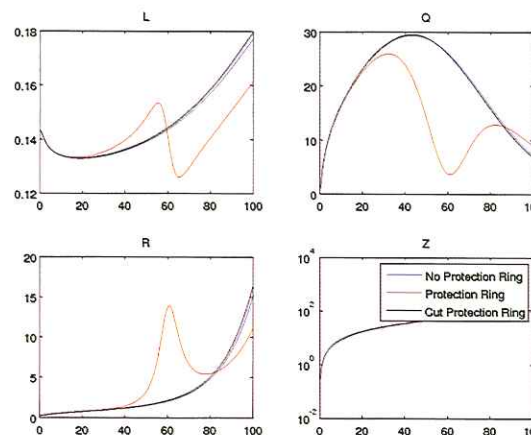
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Simulations

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- Using a guard ring shows odd behavior at higher frequencies
- The ring is a metal line of about 600um long.
- At 50Ghz the wavelength is 3000um.
- Order of a quarter wavelength line. Couples to the inductor as an LC resonator
- Removing the ring or cutting the ring fixes the issue.

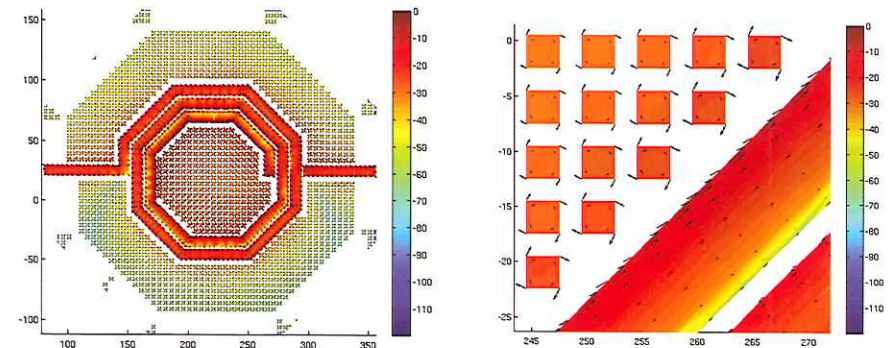


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Dummy fill simulation

Integrand
Software, Inc.



EMX models circulating currents in dummy fill.
Eddy current loss increases at higher frequencies

Not confidential/proprietary

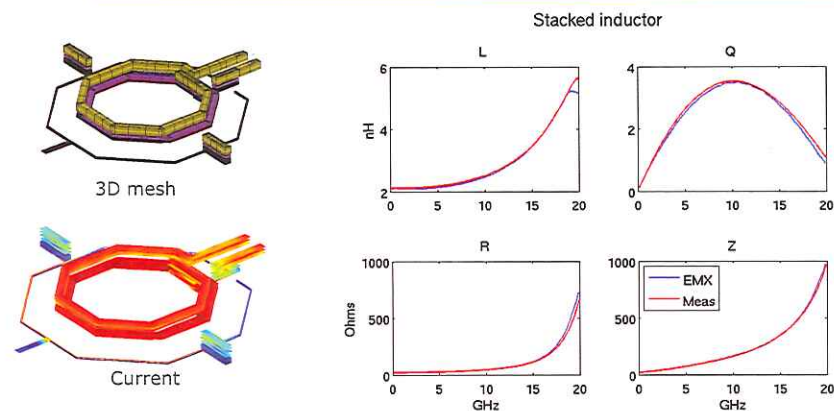
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Experimental validation

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21

Stacked inductor

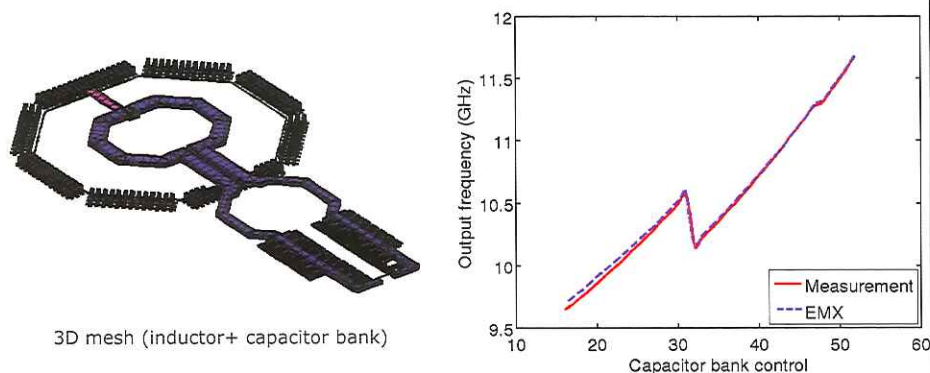


Example	Ports	Freq Range	Size	1 CPU		8 CPUs	
				Mem.	Time	Mem.	Time
Stacked Inductor	2	0.2GHz-20GHz	10,407	453MB	6m58s	688MB	4m42s

Courtesy: TSMC. 65nm RFCMOS, 9LM thick metal technology. Published at RFIC 2009
 "Including Pattern-Dependent Effects in Electromagnetic Simulations of On-Chip Passive Components", Integrand and TSMC
 Not confidential/proprietary

22

CMOS VCO



Example	Ports	Freq Range	Size	1 CPU		8 CPUs	
				Mem.	Time	Mem.	Time
CMOS VCO	20	0.1GHz-20GHz	137,694	5216MB	399m41s	18878MB	98m19s

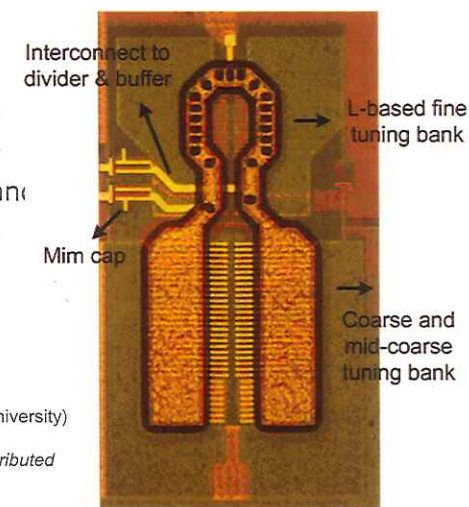
Courtesy: Wipro, TSMC90nm, 1P5M

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Complete L-DCO tank EM simulation

- Including:
 - Coarse, mid-coarse tuning bank
 - Fine tuning bank
 - Interconnection to divider and buffer
 - Mimcap for AC coupling
 - Ground ring
- 100+ port EMX simulation



W. Wu, J.R. Long, R.B.Staszewski, J.J. Pekarik (Delft University)

"High-resolution 60-GHz DCOs with Reconfigurable Distributed Metal Capacitors in Passive Resonators,"

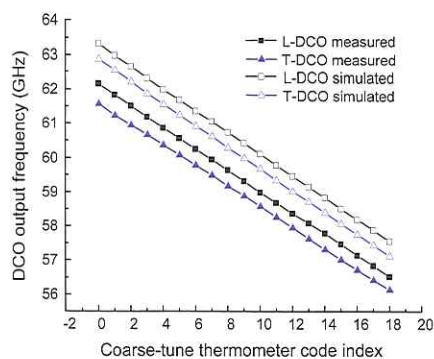
IEEE Radio Frequency Integrated Circuits Symposium, June 2012.

Not confidential/proprietary

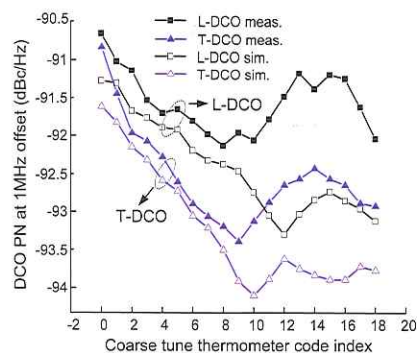
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60-GHz DCO measurements

Integrand
Software, Inc.



Measured vs.
simulated coarse
tuning curves of DCOs



Phase noise agreement

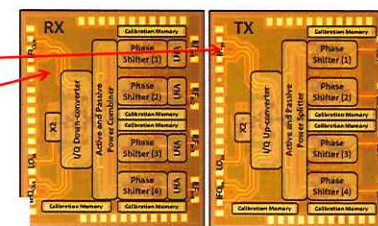
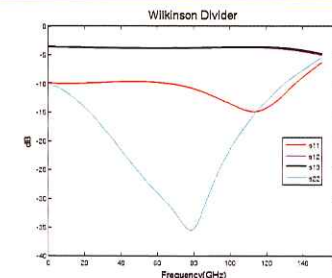
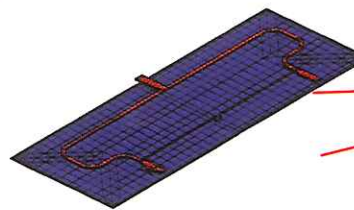
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Wilkinson Divider

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Software, Inc.

- Wilkinson Dividers can be used as power splitters and power combiners
- In silicon it is not ideal and all real effects need to be included (ground plane, resistors, etc.)
- EM simulation needed



A 70-100GHz Direct-Conversion Transmitter and Receiver
Phased Array Chipset in 0.18 μ m SiGe BiCMOS Technology
Shahriar Shahramian (Member IEEE), Yves Baeyens (Fellow IEEE), Young-Kai Chen (Fellow IEEE)
Bell Laboratories, Alcatel-Lucent, Murray Hill, NJ 07974, USA

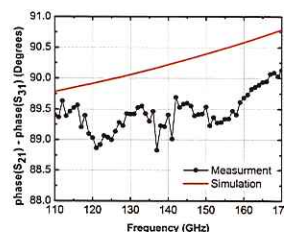
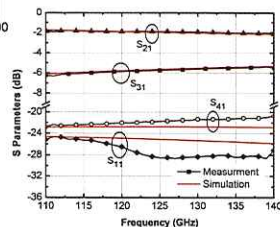
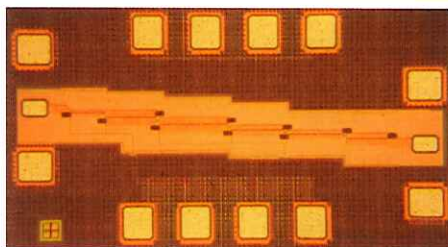
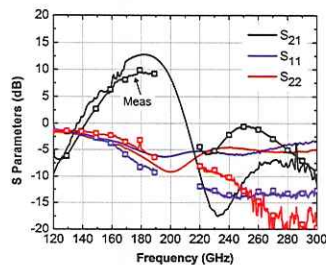
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6dB coupler and amplifier

Integrand
Software, Inc.

6 db Coupler up to 200GHz



University of Toronto

IMS 2012 (private communication)

Ionnis Sarkas, Sorin Voinigescu

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Conclusions

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- Maxwell's equations used to model passive structures at high frequencies
- Need fast 3D Full-wave EM solver to capture relevant effects
- Linear time solver like EMX
- Design issues
 - Coupling to stray lines
 - Capacitor Q degradation
 - Retardation needs to be modeling
- Circuits can and are being built for very high frequency applications

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Challenges ahead...

- Constant improvement of speed and memory use
- Cannot do full-chip level 3D EM extraction
- Better characterization of interconnect and substrate
- Packaging considerations
 - Simple RLC models for packages won't suffice (seeing this for SERDES applications 30-40GHz).
- Measurement difficulties at very high frequencies
- Improvements in measurement equipment for D-band and W-band (higher frequencies)

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Acknowledgements

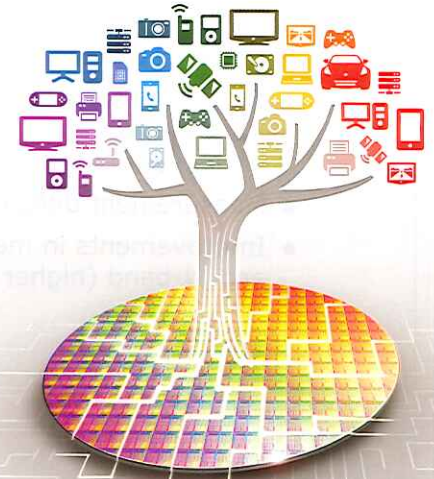
- TSMC for the circuit examples from the RFIC 2009 paper.
- TU Delft
 - Providing DCO example
- University of Toronto
 - 6dB coupler example
- Alcatel Lucent
 - W-band data link Rx/Tx example.

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Numerical Sizing for Full-Custom Designs

MunEDA

ABSTRACT

Numerical sizing is the calculation of optimal device geometries for a full-custom design, for example high-speed I/O or memory interfaces. Sizing aims at improving performance and statistical robustness, as well as reducing area or power consumption. It is a key design task in full-custom design, but is still performed manually by many designers. Numerical sizing tools like MunEDA's WiCkeD help the designer to significantly improve design efficiency and quality. In this presentation, we'll show how MunEDA's software for full-custom circuit analysis and semi-automated sizing can be used with TSMC technologies. Addressed topics include full-custom IP migration, circuit optimization, and advanced statistical circuit analysis.



MunEDA Improve Design Performance & Yield

MunEDA

Numerical Sizing for Full-Custom Designs

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MunEDA Improve Design Performance & Yield

MunEDA WiCkeD™: Tools for Circuit Designers

WiCkeD: A software tool suite for full-custom circuit designers

- Full Custom Analog & RF
- Full Custom Digital
- IP libraries, standard cells

WiCkeD contains tools for

- Design Analysis & Verification
- Design Sizing & Optimization
- Design Modeling

WiCkeD is integrated into standard design environments

- works with industrial spice and fast spice simulators

For WiCkeD customer references see <http://www.muneda.com/Customers>

Qualified for TSMC AMS Reference Flow and TSMC RF RDK

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Challenges in Full-custom Nanometer Designs

Most nanometer ICs contain critical parts that are created in a full-custom design style

Full Custom Digital	<ul style="list-style-type: none"> High-Speed I/O Memory Interfaces SRAM FPGA Core
Full Custom Analog	<ul style="list-style-type: none"> Low Power Analog RF Transceiver Equalizer PLL / VCO DC-DC Converter
Standard Cell & Libraries	<ul style="list-style-type: none"> Latches Flip-Flop Clock Buffers Inverter

Full-custom blocks are critical for

- design time,
- key performance metrics,
- and yield

Full-custom designers spend a lot of time

- analyzing
- optimizing their designs

Standard Custom IC tool suites provide

- mature tools for design entry, layout, and simulation,
- but contain only basic tools for further analysis and optimization.

MunEDA WiCkeD provides advanced tools for analysis and sizing of full-custom design and libraries

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Challenges of Advanced Node Design

➤ **Circuit sizing: Designers have to carefully set circuit parameters like W, L, R, C, ...**

- to meet performance targets
- to reduce sensitivities vs. Vdd, temperature, process, LDE, mismatch

➤ **Creating a robust design becomes more challenging in advanced nodes**

- higher sensitivity vs. supply voltage
- higher sensitivity vs. temperature
- reduced voltage headroom
- wider corner spread
- increased local variation
- layout dependent effects (LDE)

See Beacham et al. (Synopsys Inc.): "Mixed-Signal IP Design Challenges in 28 nm and Beyond". www.design-reuse.com

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Numerical Sizing in the Full-custom Design fFlow

➤ Numerical sizing is a must-have for advanced circuit design

- High-speed I/O: transients, balancing over corners
- RF: optimize noise and jitter vs power trade-offs
- Complex OTAs: speed, stability, feedback loops
- Low power analog: specs vs. power trade-off
- Memories: full-custom I/O, paths, sensing, ...

➤ Numerical sizing is critical for many products' KPI

- Ultra low power design, mobile communication, medical, near field communication, memories, FPGA

➤ Numerical sizing consumes a lot of designer's time

- Experienced designers spending weeks of interactive tweak-simulate-tweak

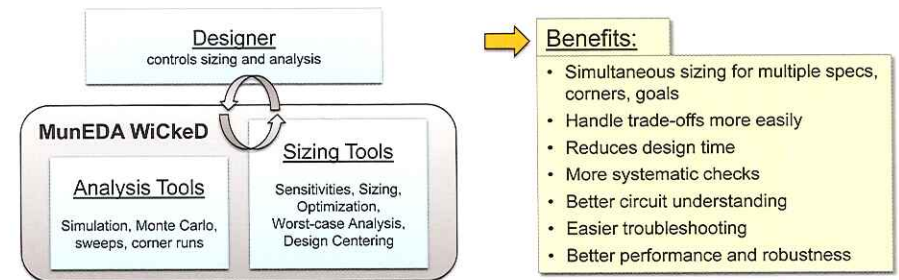
Full Custom Design Flow

➤ The standard full-custom flow provides tools for design entry and circuit analysis

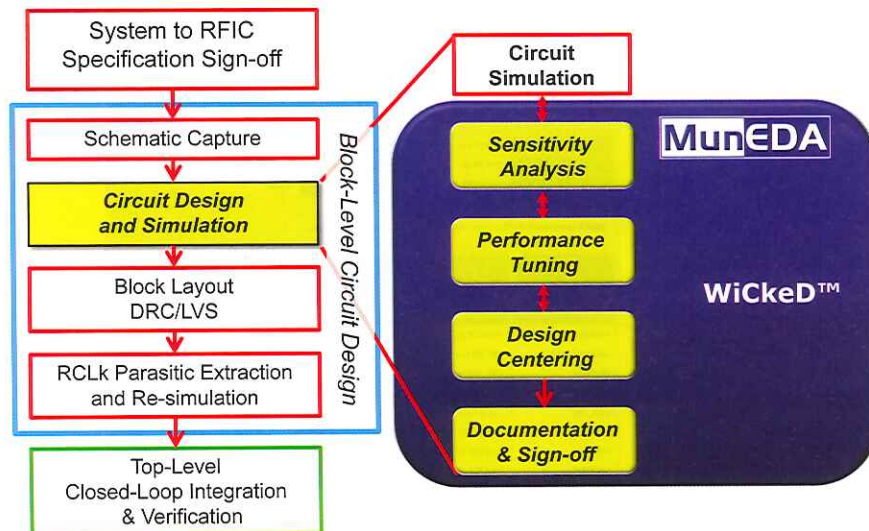
- Simulation, corner runs, Monte Carlo, LDE estimation, parameter sweeps

➤ MunEDA WiCkeD completes the flow with tools that help the designer to size the circuit for performance and robustness

- Sensitivities, Sizing, Optimization, Worst-case Analysis, Design Centering



Flow Overview: TSMC RF RDK 2.0



Sizing Solution: MunEDA WiCkeD

Traditional Approach

Manual tweak-simulate-tweak with interactive tools

High manual effort

Sub-optimal solutions for hard problems

Inefficient for repetitive tasks

No work flow documentation
Only experts with many years of experience can do it well

Solution: MunEDA WiCkeD

Integrated sizing environment with interactive and automated tools

Automated runs, designer can focus on the creative tasks

Efficient optimization that works, tuned for the difficult problems

Batch mode processing, scripted sizing strategies

Documented sizing flow

Circuit design knowledge is a must, but **junior engineers get a fair chance**

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TSMC Test Case Introduction

- Test Case description
 - **Circuit:** RF LC tank VCO,
 - **Process:** 65nm (CRN65LP)
 - **Fosc:** 2.475GHz
- Test Case validate feature
 - **Automatic Performance Tuning**
 - **Automatic Yield Optimization**
 - **Sensitivity to process variation and mismatch**

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VCO Example from TSMC RF RDK 2.0

- Original circuit performance
 - **Kvco:** 40MHz/v
 - **Phase noise :** -99dBc/Hz @ 100k
 - **Phase noise :** -123dBc/Hz @ 1M
- Step 1: Performance improvement
 - **Kvco:** 70MHz/v
 - **Phase noise :** -101dBc/Hz @ 100k
 - **Phase noise :** -126dBc/Hz @ 1M
- Step 2: Yield improvement by 50%

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65nm VCO Example from TSMC RF RDK 2.0

Performance Tuning

Phase_Noise_100K < -100

dB

Iteration count

FAIL region PASS region

Monte Carlo Analysis

WickuD - Monte Carlo Analysis (Node 11)

Phase_Noise_100K

Mean Value: -101.500 m, Min Value: -101.500 m, Max Value: -101.500 m

Standard Deviation: 0.000 m, Variance: 0.000 m

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VCO Example from TSMC RF RDK 2.0

Sensitivity Analysis

Performance: phase noise

Estimation accuracy: 99.8%

Process Parameter	Influence	Rel. Influence	Regression Coefficient (standardized)	95% Confidence Interval (standardized)		P< t
			Lower	Upper		
random3_res	190.002 m	33.3 %	0.5092	0.5985	0.6199	****
random1_min	-101.844 m	30.5 %	-0.50304	-0.5938	-0.5723	****
random2	141.382 m	18.4 %	0.45331	0.4426	0.464	****
random1	-119.527 m	13.2 %	-0.38323	-0.394	-0.3725	****
par2_ind	-51.113 m	2.4 %	-0.16388	-0.1746	-0.1532	****
par1_ind	-31.0014 m	0.9 %	-0.099399	-0.1101	-0.08867	****
random3	24.5559 m	0.6 %	0.078765	0.06884	0.08949	****
random4	24.2352 m	0.5 %	0.077764	0.06698	0.08843	****

Process parameters ranked by influence

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VCO Example from TSMC RF RDK 2.0

Topic	Conventional Design Style	Using MunEDA WiCkeD™
Specification-driven circuit design	– Uncontrolled overdesign spending area and power for random safety margins on all specs	+ Balance specs, area, power and process robustness VCO: phase noise reduced by 3dB
Circuit design re-use for new spec	– Migrate a large number of cells in pure manual labour	+ Automate sizing tasks to maximize designers' efficiency VCO: designer efficiency +50%
Circuit design for yield	– Limited analysis capabilities, guesswork, trial-and-error	+ Fast design centering in a controlled environment VCO: fully automatic yield improvement +50%

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Numerical Sizing of I/O Levelshifter in 20nm

0.85V → 1.8V I/O levelshifter in TSMC 20nm Process Technology

- **Challenge:** Sensitivity to Process variation and Vdd variation causes too wide corner spread
- **Task:** optimize MOSFET widths to reduce corner spread of duty cycle and delays
- **Result:** Fully automated sizing with MunEDA WiCkeD, easy setup, short runtime (<3min. @ 1 CPU), significant reduction in corner spread (-50%)

Benefits:

- Simultaneous sizing for multiple specs, corners, goals
- Handle trade-offs easily
- Reduces design time
- Better performance and robustness
- Works with many simulators
- Pre-layout and post-layout netlists
- Batch-mode capable

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SRAM Bitcell High-sigma Worst-case Analysis in 20nm

SRAM bitcell in TSMC 20nm Process Technology

- **Challenge:** Verification for sensitivity to local variation
- **Task:** Calculate worst-case condition in a 5 sigma range of mismatch parameters
- **Result:** short runtime (<2min. @ 1 CPU), easy setup, shows sensitive parameter subset, writes worst-case netlist

Performance	Specification	Analysis	Worst-Case Distance
ICELL	> 2.6578	←	5.800

Name	Value
XMPD0/PARL1_SR	-
XMPD0/PARL2_SR	-
XMPD0/PARL3_SR	-
XMPD0/PARL4_SR	-
XMPD0/PARL5_SR	-
XMPD1/PARL1_SR	-
XMPD1/PARL2_SR	-
XMPD1/PARL3_SR	-
XMPD1/PARL4_SR	-
XMPD1/PARL5_SR	-
XMPG0/PARL1_SR	-
XMPG0/PARL2_SR	-
XMPG0/PARL3_SR	-
XMPG0/PARL4_SR	-

Benefits:

- Handles non-linearities and long-tail non-Gaussian distributions
- Fast
- Supports many simulators
- Batch-mode capable
- Output useful for interface optimization (sensing, ...)

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Further References

- **Industrial application cases from MunEDA User Group Meetings**
 - Calculate optimal PLL system parameters in behavioral models considering process variation
 - Area reduction in lookup tables (2.5k MOS, 30k RC, 190 parameters)
 - Reduce noise and power consumption of RF receivers (2k MOS, 8k RC)
 - Reduce process sensitivity of memory interfaces (DRAM, NVM, SRAM, ...)
 - Optimize libraries of clock buffers and latches
 - Low power analog sizing (OTA, PHY, ...)
 - many more ...

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IP Migration

- Many full-custom blocks in nanometer designs are re-used and enhanced versions of existing designs.
- A lot of full-custom IP has to be migrated between processes
 - Fab migration: going fabless, changing supplier
 - Process migration: going to the next node)
 - IP libraries: offering multiple options
- Migrating full-custom designs often requires modifications, resizing, and verification in the frontend, before creating the new layout
- Efficient full-custom IP migration is key for nanometer design success

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MunEDA Full-Custom Frontend IP Porting Workflow

The generalized design flow follows 3 major steps

1. Schematic Porting or IP Re-use
2. Design Assessment (Analysis & Verification)
3. Sizing & Sign-off (Circuit Optimization: Sizing and Design Centering)

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Summary

- Advanced technology nodes pose new challenges for robust full-custom design with high parametric yield.
- MunEDA provides tools for analysis and optimization of full-custom designs and libraries/IP, with the goal of reducing design risk and improving productivity.
- TSMC and MunEDA cooperate on RF and Full-Custom Reference Flow.
- Optimization results of a 65nm RF VCO and 20nm I/O cell were shown, as well as high-sigma robustness analysis of a 20nm SRAM bitcell.

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NOTE

This image shows a single sheet of white paper with horizontal ruling lines. The lines are evenly spaced and run across the width of the page. There are no margins, text, or other markings on the paper.

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From the Cell to the System: Variation-Aware Memory Design at 28/20nm

Solido Design Automation



ABSTRACT

This talk describes the Solido variation-aware memory design tools, that are part of TSMC's newly updated custom reference flow for 28nm and 20nm. It includes High Sigma Monte Carlo for memory cells, which enables designers to analyze billions of Monte Carlo samples in minutes, with full SPICE accuracy. The flow also includes Solido's new System Memory tool, which allows designers to measure yields of whole memory columns or arrays in a fast yet accurate fashion. The system tool reconciles the tradeoff between bitcell read current and yield, and sense amp offset voltage and yield, in a non-pessimistic and arbitrarily nonlinear fashion, to return a tradeoff between overall system timing spec and yield. This talk goes on to describe the silicon success that TSMC has achieved, in using Solido cell-level and system-level memory design tools in its internal flow as a customer of Solido. Results are presented on TSMC 28nm and 20nm processes. Solido tools, combined with TSMC PDKs / flows, allow memory designers to do fast, accurate, and variation-aware design at both the cell and the system levels.



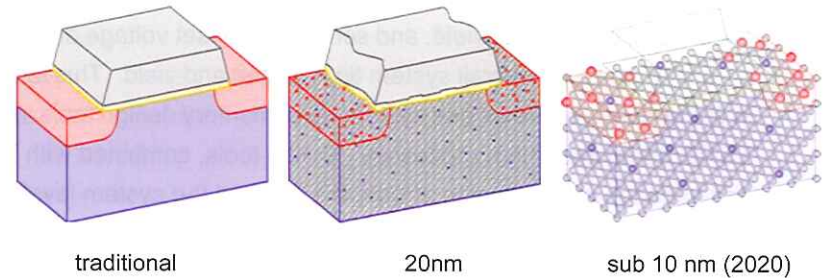


From the Cell to the System: Variation-Aware Memory Design at 28/20nm



Variation starts at the transistor level

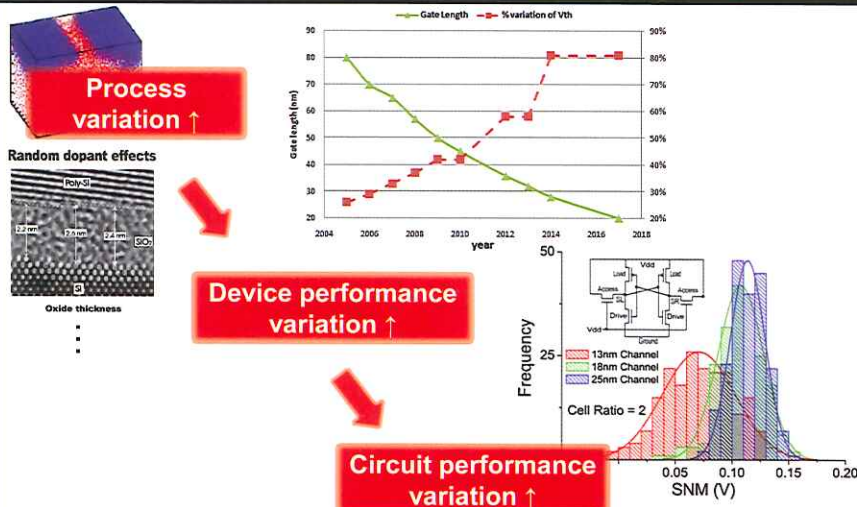
- Transistors are shrinking, but atoms are not
- Parametric variation increases with smaller devices



A. Asenov, "Statistical Nano CMOS Variability and Its Impact on SRAM", Chapter 3, A. Singhee and R. Rutenbar, Eds., Extreme Statistics in Nanoscale Memory Design, Springer, 2010



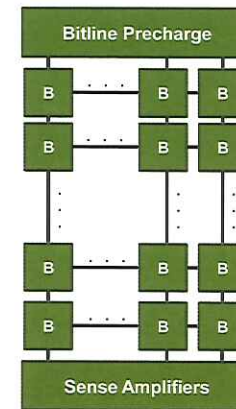
Increasing variation at the transistor-level leads to significant variation at the bitcell



-A. Asenov, "Statistical Nano CMOS Variability and Its Impact on SRAM", Ch. 3, A. Singhee and R. Rutenbar, Eds., Extreme Statistics in Nanoscale Memory Design, Springer, 2010
-C. Visweswariah, "Mathematics and Engineering: A Clash of Cultures?", IBM, 2005
-ITRS, 2006



Increased cell-level variation requires careful trade-off analysis at the system-level



Consider a 256Mb SRAM:
→ 256M bitcells
→ 64k sense amps
→ 4k bitcells / sense amp

For the SRAM to yield, need:
Bitcell sigma $\sim 6\sigma$
Sense Amp sigma $\sim 4.5\sigma$

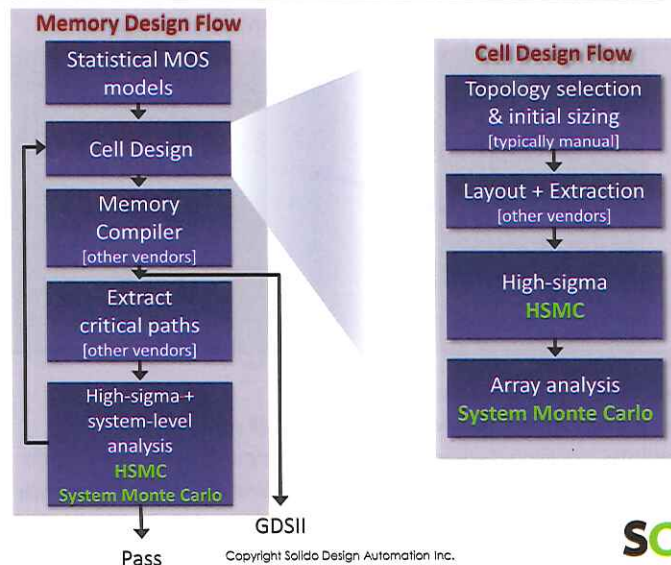
Would take **billions** of Monte Carlo simulations at the cell level, or **years** of simulation at the system level

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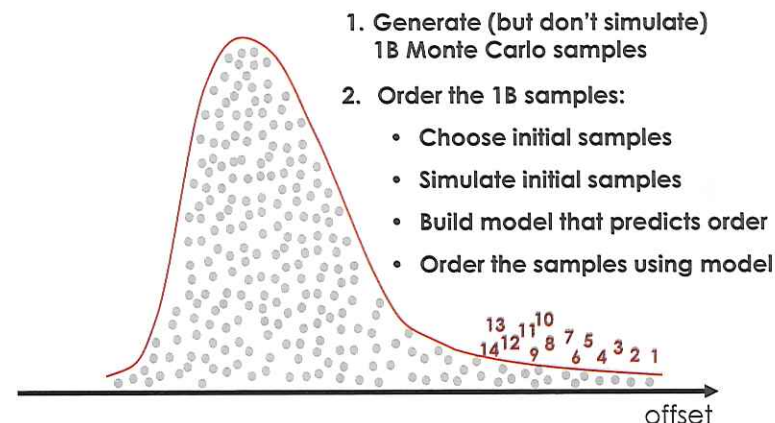
Solido Variation Designer

Faster Monte Carlo in the memory design flow



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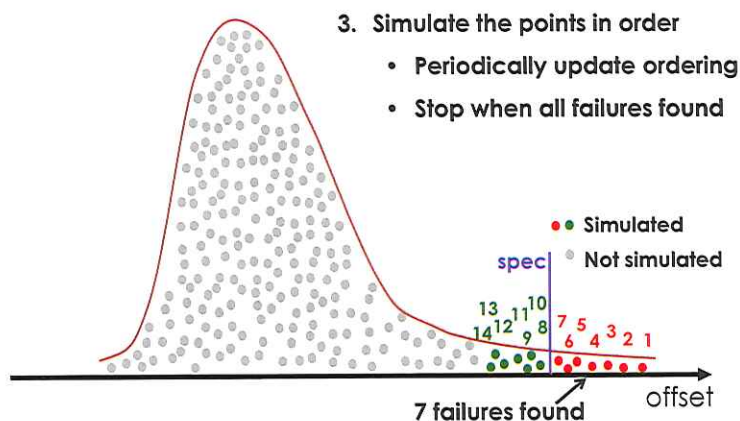
Solido High-Sigma Monte Carlo: How It Works



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Solido High-Sigma Monte Carlo: How It Works

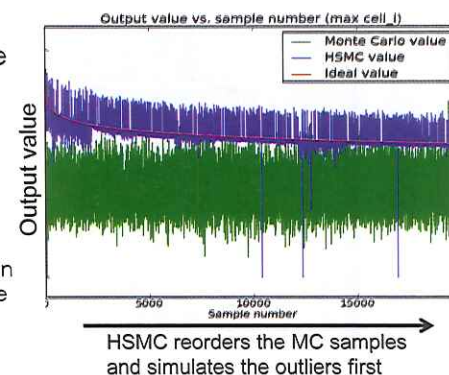


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HSMC prioritizes the MC sample to simulate

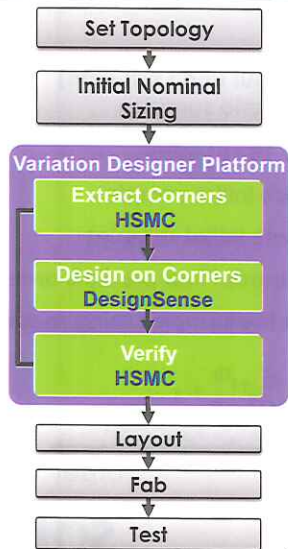
- HSMC focuses simulation resources on the tails of the output distribution first
 - All results are validated with SPICE
- Accurate prediction isn't necessary as result quality is easily verified
 - With a tough circuit, simply run longer to capture more of the tail
- During analysis, HSMC periodically updates the simulation order
 - Learns from simulation results as they are generated
- Provides visual verification of quality convergence



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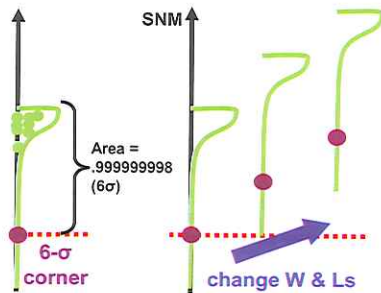
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Size designs across high-sigma corners



HSMC Benefits:

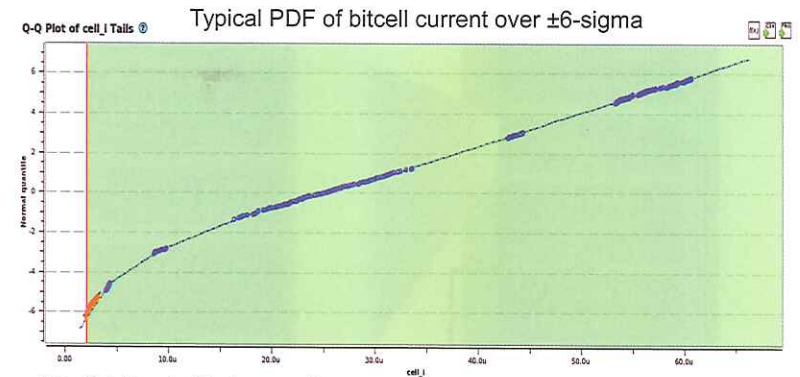
- Accuracy: As accurate as doing 1B MC simulations
- Fast: <10K sims, parallelizable
- Scalable: >1000 parameters
- Verifiable: Easy to adopt / trust



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Extract the full PDF with HSMC



- Uses full Monte Carlo sampling
- Focuses simulation resources to catch all tail samples
- Simulates additional samples to build an accurate PDF to ± 6 -sigma
- PDF is automatically available for system-level Monte Carlo analysis

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Comparison of methods for high-sigma analysis

Method	Fast	Accurate	Scalable	Verifiable
20k MC	Yes	No	Yes	Yes
1Billion MC	No	Yes	Yes	Yes
1M MC + Extrapolation	No	No	Yes	No
Worst-Case Distance (WCD)	Yes/No	No	Yes	No
Importance Sampling (IS)	Yes	Yes/No	No	No
WCD + IS	Yes/No	No	Yes	No
Solido HSMC	Yes	Yes	Yes	Yes

- Verifiability is an important criteria in evaluating accuracy and establishing confidence in any high-sigma solution

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Solido System Monte Carlo

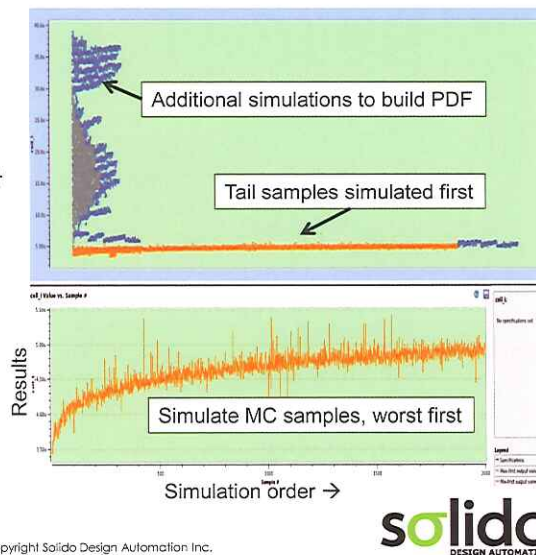
- Using the measured characteristic of sub-cells it is possible to run Monte Carlo on a higher level of abstraction to assess system performance and yield.
- Steps for using System Monte Carlo in memory design:
 - Configure the memory design with number of number of bitcells per bitline, number of sense amps and any redundancy
 - Include loading capacitance, timing goals
 - Load cell-level characterization databases
 - Run Monte Carlo analysis across the array to 3-sigma
- Fast enough to explore tradeoffs between read time and yield
 - Easily explore the impact of different architectures on yield

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HSMC analysis on a 6T bitcell

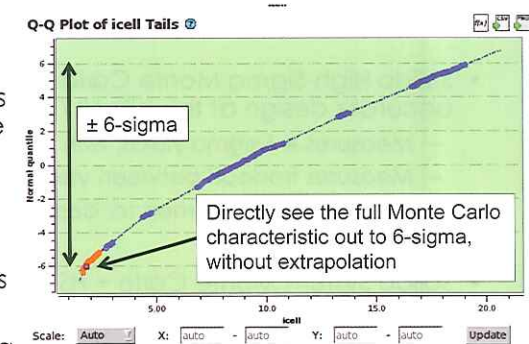
- 10,000,000,000 Monte Carlo samples are generated to validate to 6.1 sigma
- 2,000 simulations ran at the tail of the distribution
- 3,950 additional simulations to build full Probability Density Function (PDF)



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HSMC results for the 6T bitcell

- Example PDF for bitcell read current across ± 6 -sigma
- Linear extrapolation from a smaller Monte Carlo analysis will fail to predict the real 6-sigma current
- HSMC is the only solution to run full Monte Carlo analysis
- Easily extract 6-sigma samples for use as design corners

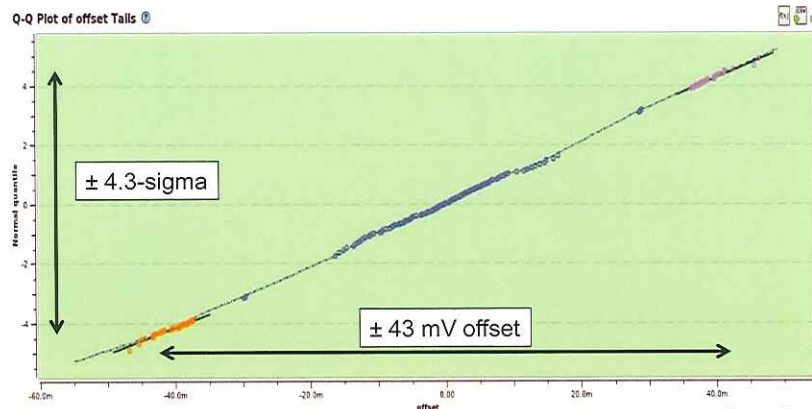


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HSMC results for a sense amp

- Ran across one million Monte Carlo samples for ± 4.3 -sigma
 - 500 simulations at each tail, 1200 simulations to build full PDF



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Solido System Monte Carlo Developed in collaboration with TSMC

- Very-fast system-level Monte Carlo analysis
- Uses full PDFs from bitcell and sense amp characterization
- Example:
 - Analyzed a 64Mbit array (16k x 4k) with 60fF bitline load

Timing spec	Column yield with confidence interval (%)	System yield with confidence interval (%)
400ps	99.9059 [99.9025, 99.9091]	1.985e-5 [1.141e-5, 3.390e-5]
450ps	99.9792 [99.9776, 99.9807]	3.3029 [2.5321, 4.2263]
500ps	99.99536 [99.99456, 99.99604]	46.765 [41.031, 52.287]
550ps	99.99863 [99.99816, 99.99897]	79.851 [74.004, 84.521]
600ps	99.999695 [99.999438, 99.999834]	95.122 [91.206, 97.320]
650ps	100 [99.999883, 100]	100 [98.097, 100]

Actual results will vary with cell design and array architecture

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Summary

Solido provides a complete Monte Carlo solution for Memory design at the cell and system level, with greater than 100x improvement in simulation efficiency

- Solido High-Sigma Monte Carlo (HSMC) enables fast and accurate design at the bitcell / sense amp Level:
 - Measures 4-6 sigma yields, with Monte Carlo and SPICE accuracy
 - Measures tradeoff between yield and read current / offset voltage
 - Extracts 6-sigma corners for design optimization
- Solido System Monte Carlo + HSMC enables fast and accurate design at the system level:
 - Measures 2-4 sigma yields of system, with SPICE accuracy
 - Measures tradeoff between timing and yield
 - Easily explore the impact of different architectures

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A Breakthrough in Logic Design Drastically Improving Performances from 65/55 nm LP and Below

Dolphin Integration

ABSTRACT

At 65/55 nm and beyond, the complexity of SoC's results in a drastic rise in the amount of storage embedded within logic blocks. Such storage is typically made of Registers, Look-Up Tables, and FIFO's - scattered in the middle of standard-cell based logic islets. Due to RTL Engineering styles, DFT considerations and physical implementation methodologies, logic designers traditionally tend to prefer a synthesizable, standard-cell-based implementation for such storage elements. Register Files have thus been reduced to small capacity sRAMs. Even if this exclusive focus of implementation may prevent them from reaching top performances in their designs.

This presentation introduces a complete and unique solution namely LogiWare for RTL Engineering, which enables to transcend these barriers at all steps of the design flow from RTL description, to Netlist, and to GDSII. Logic designers now have the possibility to make a rational selection either by:

- Synthesizing registers with the sequential components of their standard cell library
- Replacing seamlessly registers by the block-busting "Register Packs" instantiated from a brand new kind of memory compiler - CARME

Thus paving the way to the ultimate optimization of logic islets.

LogiWare and CARME are particularly needed for application processors, wireless connectivity, portable consumer, cellular baseband devices or any other application in needs for multiple memory registers.

At TSMC 65/55 nm LP for example, using CARME provides the capability to divide output delays of registers by more than 5X! The side benefit is that CARME also improves density of registers by at least 2 times and dynamic power consumption by more than 5...

LogiWare and CARME can be easily ported to any process node and flavor.

LogiWare includes:

- A library of VERILOG models of registers
- The SESAME HD standard-cell library, unique Reduced Cell Stem Library (RCSL) with its track-compatible HS extension
- The CARME memory compiler which breaks the traditional limitations of synchronous memories acting exactly as synthesized registers, and featuring the shortest possible output delay for speed-critical elements such as Look-Up-Tables
- Several efficient scripts for automatic detection of registers in a RTL design and their swift replacement by a model enabling both synthesis and instantiation of registers


This presentation provides insights into three main topics:

The first one introduces the different LogiWare components including the unique, and patent-pending CARME architecture. It further describes how the combination of SESAME standard cell library, VERILOG models and CARME memory generator presents for the first time a complete flexibility of logic design implementation – from standard cell based implementation up to custom memories while maintaining the basic features of RTL design and functionality.

The second topic of this presentation addresses the challenge of implementing DFT for SRAM-Based registers, and it presents CARME's patent-pending scan test technology.

The third topic actually demonstrates through benchmark results how logic designers can leverage both TSMC 65/55 nm LP process and LogiWare for optimizing and structuring such widespread loose pieces as scattered registers, register files and Look-Up-Tables into structured register packs.






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A breakthrough in logic design drastically improving performances from 65/55 nm LP and below

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Agenda

1. About Dolphin Integration
2. Market trends
3. Challenges for logic designs from 65/55 nm and below
4. How to improve performance of standard cell libraries
5. RCSSL Booster components highlight
6. Summary

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Corporate ID


- Incorporated as French SA in 1985
- on Alternext of NYSE in 2007
- as the provider of design products for mixed signal SoCs
- now active from 180 nm to 28 nm
 - with 135 Design Engineers
 - plus Field Application Engineers and SoC Integration Engineers expert at Hardware Modeling to provide SoCs with the best subsystems:
 - High Resolution Audio (Converters and Audio Signal Processing)
 - High Resolution Measurement (Converters for Power Metering, Mems, etc.)
 - Low-power Storage (Register Banks and Memories)
 - Low-power Microcontrol Logic (80x51 Legacy, eFlash Caches, Coprocessors...)
 - and innovative libraries of Standard Cells and Memory Registers
 - with Power Regulation, Reference, Clock & Detector Networking
 - where the major differentiator is the Flexibility of IP configurations (FLIP)



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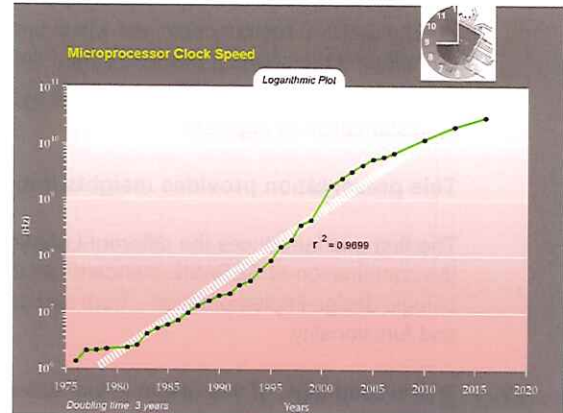


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Market trends: Boom of average SoCs clock speed

- Consumer electronics and mobile devices drive the need for higher SoC performances
 - High performance required for embedded processor
 - High density and low power required for rest of SoC
- Targeted applications
 - Smartphone
 - Multimedia
 - Gaming
 - Computing
 - ...



Source: Kurzweil

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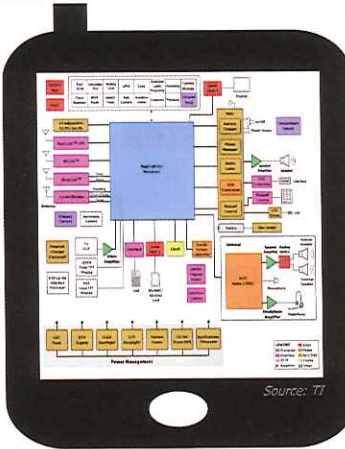


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Smartphone requirements

- More and more integrated features: touchscreen, video, gaming, GPS...
- "All-in-one" trend involving
 - Higher processing power**
 - Higher density for the complete circuit
 - Longer battery lifetime both in operation and stand-by mode
 - Low-cost packaging
- Impact at logic block level
 - High performance requirements**
 - Rise of the logic block size and amount of storage
 - Support for advanced power management techniques



Source: TI

Smartphone requires standard cell libraries delivering the performance needed for connectivity features together with low power consumption for an extended battery life!

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Challenges for logic designs from 65/55 nm and below

Market needs for higher processing power is made more complex by


- Routing complexity, Congestion
- VT selection, Trade-Off Speed/Leakage
- Temperature inversion
- Power consumption
 - Dynamic consumption
 - IR Drop & Peak-Current control
 - Static consumption
- Design for Yield
 - Process variation
 - Mismatch

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How to improve performance of standard cell libraries

- 65/55 nm SoC designs enable implementations with tens of millions of gates
 - Need for a hierarchical structure with islets as all blocks do not have the same requirements for speed, density, dynamic power, and leakage
- Logic designers can leverage 3 solutions to improve performances of logic blocks while maintaining the best density/power trade-off
 - TSMC processes and VT variants
 - Mainstream design techniques for speed optimization of standard cell libraries
 - RCSL BOOSTER by Dolphin Integration for speed optimization of standard cell libraries



Logic block A
Low frequency block
High Density library for core and power saving

Logic block B
High frequency block
High Density library for core and power saving

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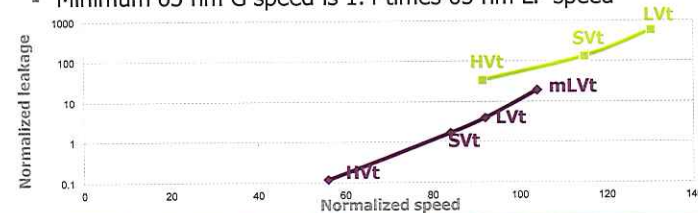
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Option #1: leverage TSMC's processes

- Balancing low power and high performance at 65 nm with TSMC process options
 - Wide range of transistor variants
 - Wide range of process variants
- 65 nm leakage/speed comparison
 - Minimum 65 nm G leakage is 30 times 65 nm LP leakage
 - Minimum 65 nm G speed is 1.4 times 65 nm LP speed

Standard Offering	GP	LP	ULP	LPG	
				LP	G
Vdd(V)	1	1.2	1	1.2	1
Vt	Low	●	●	●	
	Medium Low		●		
	Standard	●		●	●
High	●	●	●	●	

Source: www.tsmc.com




Normalized leakage

Normalized speed

Legend: TSMC 65 nm G (yellow line), TSMC 65 nm LP (purple line)

Labels on graph: HVT, SVt, mLVt, LVT, SVt, HVT

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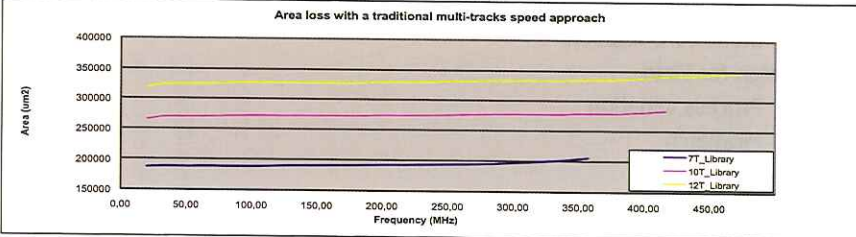


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Option #2: leverage mainstream design techniques for speed optimization

Design techniques	Drawbacks	Impacts
Cell paths optimization: identify and reduce the critical paths of the cells. Especially relevant for complex cells (eg. Adder, half-adder)	Field of actions reduced on simple cells. More concerned for complex cells, not necessarily used in critical paths. Trade-off with the drive strength needs to be addressed.	AREA LOSS
Multi track: selecting 7/8 Track libraries for density optimized blocks and 10/12/14 Track libraries for speed critical blocks.	Most libraries are not path mixable, so optimization is limited to the whole logic block level: cells are oversized for all non-critical paths of the block.	AREA LOSS
Mix VTs: Lvt in critical path and Hvt-Svt in non critical path.	An additional LVT layer is needed. The important leakage of LVT cells.	LEAKAGE LOSS

Area loss with a traditional multi-tracks speed approach



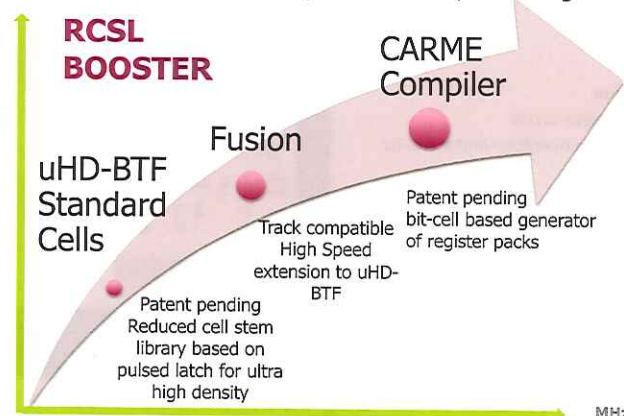
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Option #3: leverage Dolphin's RCSL Booster for speed optimization

The alternative to traditional design techniques to reach the optimum between performance, density, and power consumption of logic blocks



LogiWare models


Library of verilog models of registers

Scripts

Automatic detection of registers in a RTL design and their swift replacement by a model enabling both synthesis and instantiation of registers

RCSL Booster optimizes logic designs at three levels: RTL, Netlist, GDSII

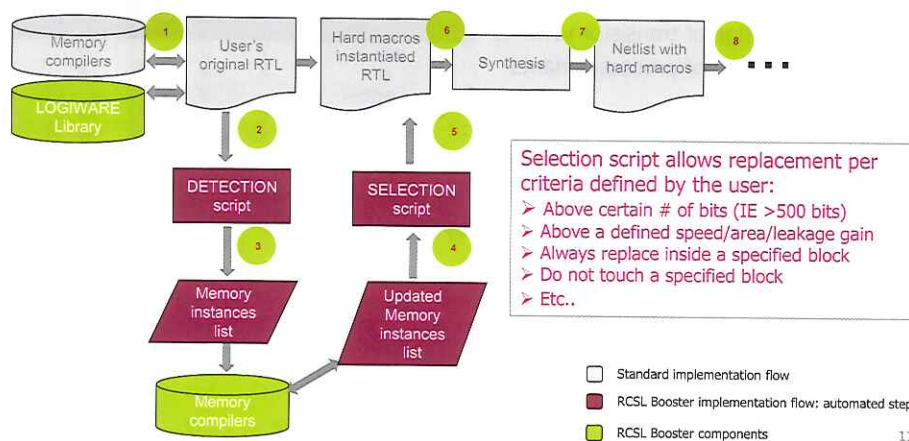
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Option #3: leverage Dolphin's RCSL Booster for speed optimization


Optimization process with RCSL Booster



Selection script allows replacement per criteria defined by the user:

- Above certain # of bits (IE >500 bits)
- Above a defined speed/area/leakage gain
- Always replace inside a specified block
- Do not touch a specified block
- Etc..

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Option #3: leverage Dolphin's RCSL Booster for speed optimization

Benchmark: Implementation of a 16x16 Look-Up-Table (TSMC 65nm LP)

Property/Challenge	Synthesizable FF-Based	Synthesizable Latch-Based	SRAM-Based	CARME Register Pack
Area (65LP)	3973 um²	1965 um²	1530 um²	2704 um²
Speed (access time, typical)	0.39 ns	0.6-0.8 ns	0.8-1.0 ns	0.22 ns
Power @1GHz	2.03 mW	0.80 mW	1.43 mW	0.89 mW
Reset	Yes	Yes	No	Yes
Write access	Synchronous	Synchronous	Synchronous	Synchronous
Read access	Asynch.	Synchronous	Synchronous	Asynch.
Multi Port	Yes	Yes	No	Yes

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**RCSL Booster components
highlight: Fusion**

- RCSL approach versus traditional standard cell library
 - Traditional libraries, classified as “Complex Cell Set Libraries” (CCSL), are unstructured bundles of cells and functions trying to satisfy at once several optimization criteria: speed, power, leakage, area...
 - Fusion is an add-on to the uHD-BTF which is a Reduced Cell Stem Library (RCSL) which stars only few dozens of functions for truly handcrafted cells
- Benefits
 - Diversity of optimizations to address any SoC requirements
 - High Density, Low Dynamic Power, Low Leakage or High Speed through fusion
 - Highest value through careful optimization of each cell at both electrical and layout levels
 - Proven by relevant benchmarks

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**RCSL Booster components
highlight: Fusion**

- Fusion extends the SESAME uHD-BTF library by boosting its speed
- Approach
 - Mixable cells from SESAME uHD-BTF library and SESAME HS add-on
 - Library stem cells are freely and automatically mixable within a timing path
 - Same power line rails
 - Optimization can be performed within and between blocks
- Benefits
 - Optimized performance
 - Simple, double and triple heights for ultimate flexibility
 - Additional drives on specific cells
 - Special cell design for HS add-on

With Fusion, logic designers can not only mix Vts and Simple, Double libraries but also have the unique possibility to mix them with Triple height libraries!

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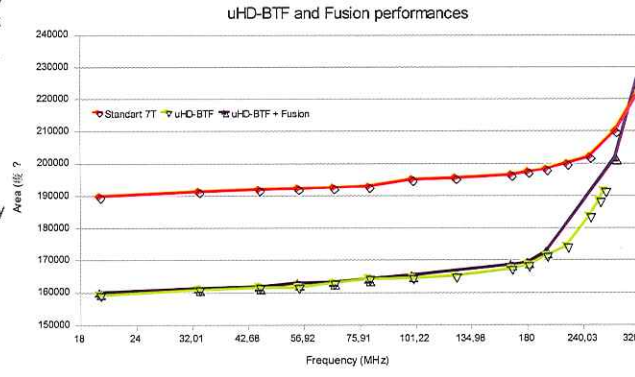


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**RCSL Booster components
highlight: Fusion**

- Principle
 - Save power and area by using SESAME uHD-BTF only on timing relaxed logic block
 - Up to 10% denser than standard 7-Track library at 65/55 nm
 - When SESAME uHD-BTF does not reach the speed constraint, mixing HD and HS cells will improve performance as the synthesizer will automatically use HS cells only on the critical paths of the speed sensitive block
 - Fusion enables to increase the maximum speed by 30%


uHD-BTF and Fusion performances



Frequency (MHz)	Standard 7T Area (µm²)	uHD-BTF Area (µm²)	uHD-BTF + Fusion Area (µm²)
18	190000	160000	160000
24	190000	160000	160000
32.01	190000	160000	160000
42.68	190000	160000	160000
56.92	190000	160000	160000
75.91	190000	160000	160000
101.22	190000	160000	160000
134.98	190000	160000	160000
180	190000	160000	160000
240.03	200000	170000	160000
320.09	230000	200000	170000

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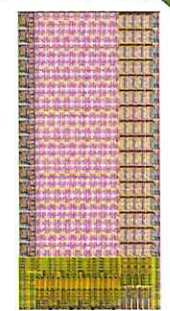
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**RCSL Booster components
highlight: CARME compiler**


- Architecture
 - Based on patentable bit-cell
 - Optimized for easy & risk-free integration within standard-cell rows
- Flexibility
 - 2 to 128 words
 - 4 to 144 bit wide
 - Up to 4 independent read-ports
- Features & Benefits
 - Very fast asynchronous read operation
 - Synchronous write
 - 1 write port, multiple read ports
 - Reset function
 - Retention Mode
 - Byte/Bit-Write control



CARME register pack
16X16
TSMC 65LP
Access time 220ps

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Summary

- Complete solutions to address your integration challenges
 - RCSL BOOSTER is the optimal solution to meet your SoC performance targets in the smallest area, achieving high performance using high-density and low power libraries
 - CARME is an innovative patent-pending breakthrough in logic design combining the flexibility and testability of synthesizable registers together with the high density of memory generators and the high speed of custom data-paths
- Dolphin integration is continuously challenging the traditional library market with the introduction of patented ground-breaking innovations allowing SoC architects and backend-engineers to maximize their silicon performance/cost.



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Charge-Trapping OTP Memory for Low-Voltage and Low-Power Operations with Superior Reliability and Testability

NSCore



ABSTRACT

A unique charge-trapping OTP memory technology has been developed in 0.18-um to 65-nm TSMC processes and passed TSMC's IP9000 qualification process. Low-voltage operations and small macro footprint have been achieved with a differential bit-cell and sense-amplifier architecture. Unlike conventional anti-fuse technologies readily available on the market today, every transistor and node in the charge-trapping OTP cell is testable without the need to program the bit cell.

The paper will present targeted applications, technical requirements and technical details for this OTP technology. The paper will also elaborate on how NSCore cooperated with TSMC IP qualification team through TSMC's IP9000 program to ensure NSCore OTP meets customers' high quality requirements.

The *hot-carrier effect* in semiconductor device physics is well known and has been deeply researched. Due to the deep understanding of the behavior of the hot-carrier effect that has been gained over the last quarter century, the phenomena is a perfect vehicle for a one-time programmable NVM. The technology presented in this paper describes how the trapped charge from the hot-carrier effect is used to program data in the bit cells of the OTP extremely reliably and predictably. When programming data, the drain node of the OTP cell is biased at approximately 5.5V. Electrons flowing from the source to the drain in a NMOSFET gain extremely high energy when drifting in a high electric field near the drain edge. A substantial number of these electrons are injected into the side-wall spacer and are trapped. The charged electrons increase V_t and decrease drain current for the NMOSFET. These trapped electrons are very stable even at a high-temperature.

The OTP memory presented in this paper has several advantages over the conventional OTP technologies.

- Field programmable with full 'pre-programmed' test coverage
- Low voltage operation (down to 0.8V)
- Low programming voltage, removing any need for added ESD protection in target circuit design
- Invisible and undetectable memory contents
- Small macro footprint





Charge-Trapping OTP Memory for Low-Voltage and Low-Power Operations with Superior Reliability and Testability

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Outlines

- Program and Read Mechanism
- Inherent Stability and Benefits to Charge-Trapping OTP
- Testing Methodology
- OTP IP Lineup in TSMC Processes
- Application Examples
- Roadmap
- Summary

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Program and Read Mechanism

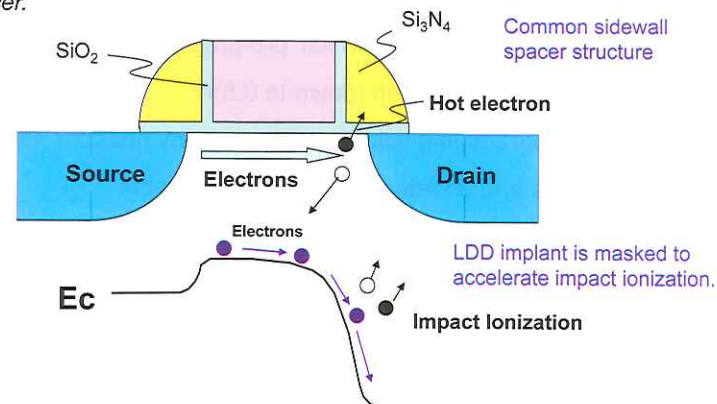
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Programming Mechanism

When nMOSFET turns ON, hot-electrons are generated and trapped in side-wall spacer.



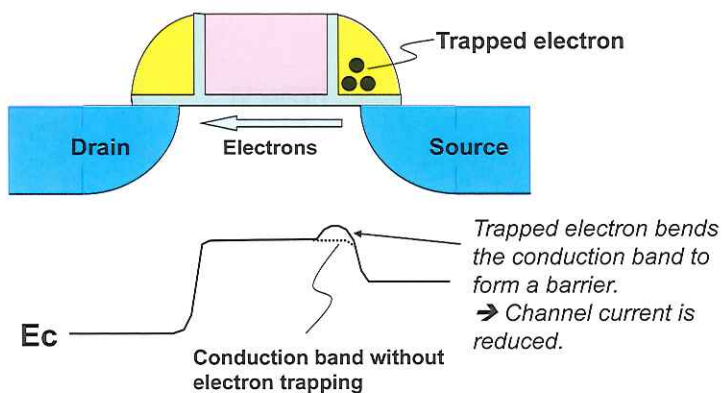
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In Read Operation

"Source" and "Drain" are reversed from Program Operation



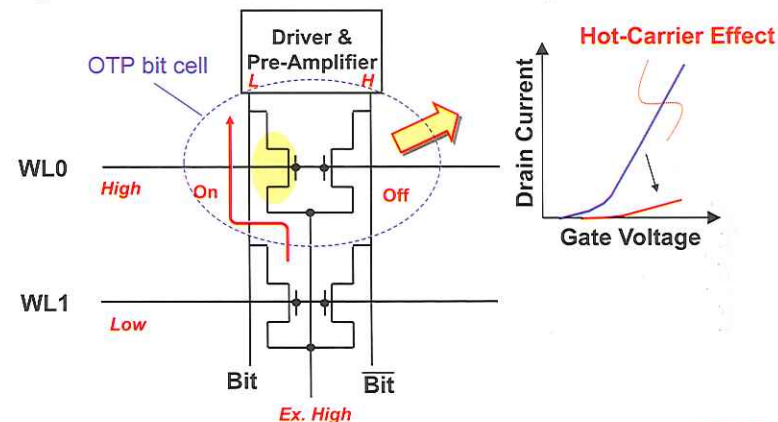
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Program Operation

Program current flows in one transistor in a cell and generate hot-carriers.



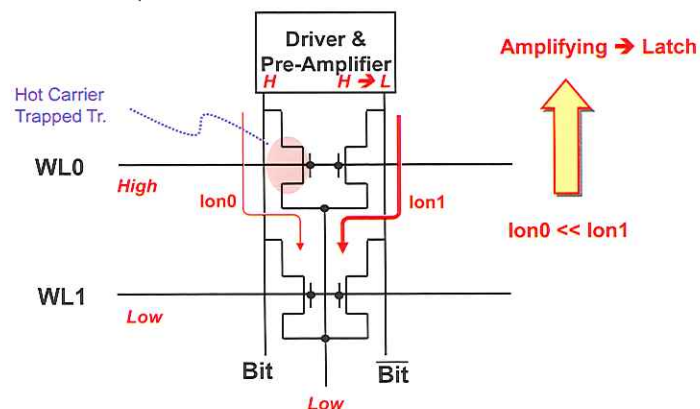
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Read Operation

Both bit-lines are pre-charged and current flows through selected cell transistors.
→ Sense amplifier senses current difference and latches.



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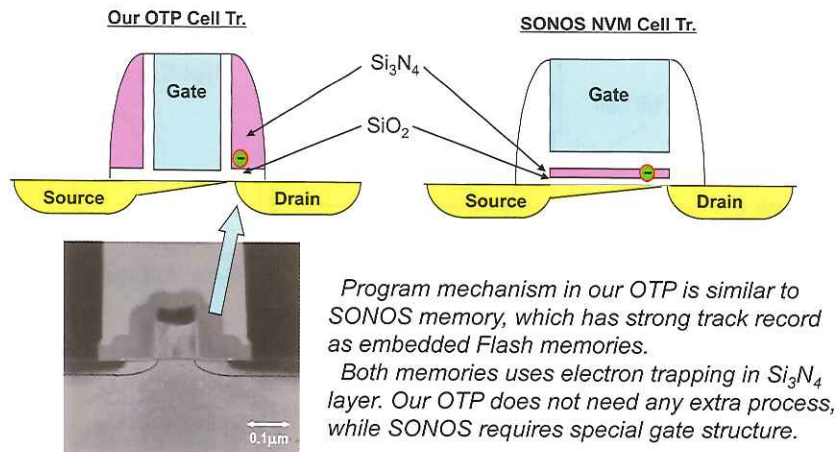
Inherent Stability and
Benefits to Charge-Trapping
OTP

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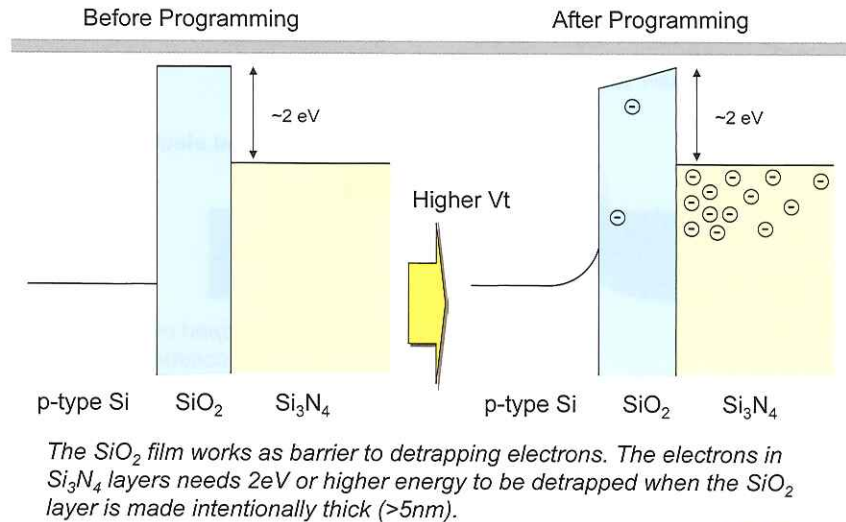
Similarity with SONOS Memory



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Detrapping Mechanism

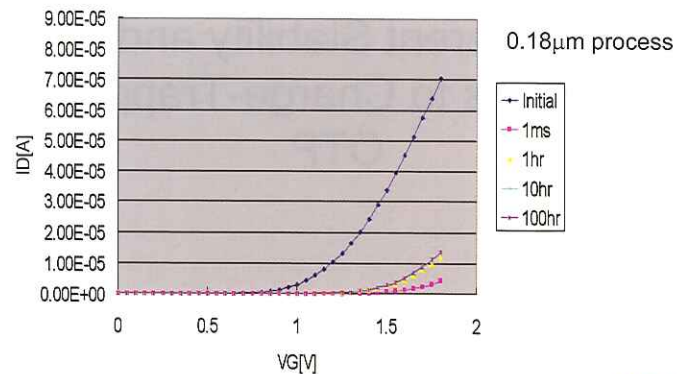


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Excellent Retention Characteristics

The cell current was drastically reduced and has been stable even after baking for 100 hours at 200°C , which is equivalent to over 30 years at 125°C .

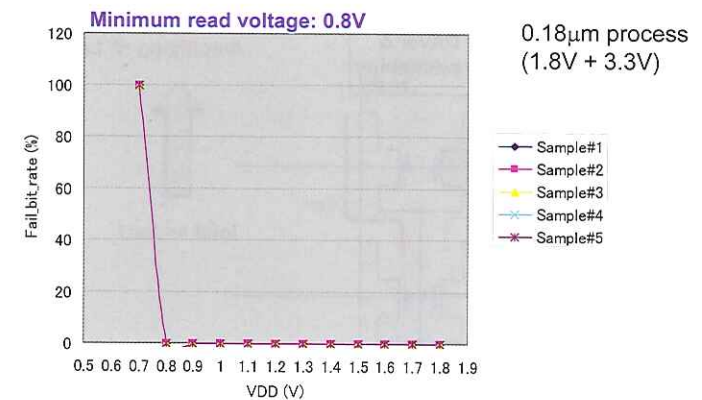


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Low-Voltage Read

Differential cell structure supports low-voltage and low-power read operation.



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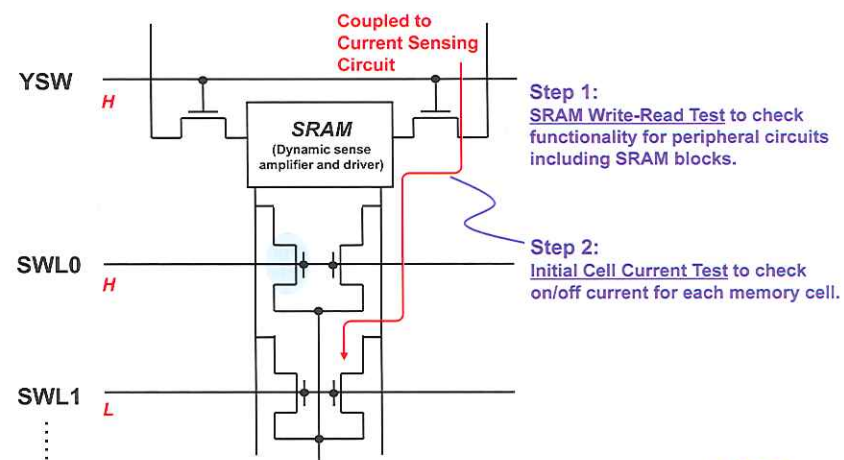
Testing Methodology

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Step 1 & 2 (before programming)

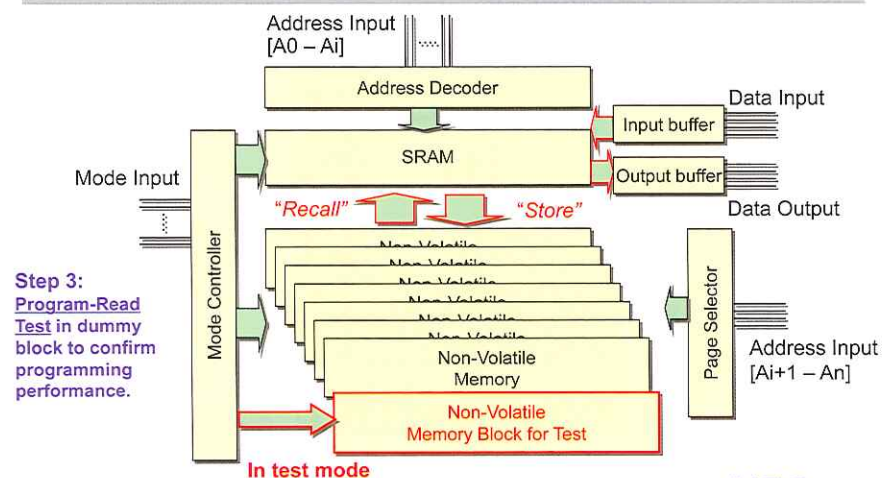


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Step3 (before programming)

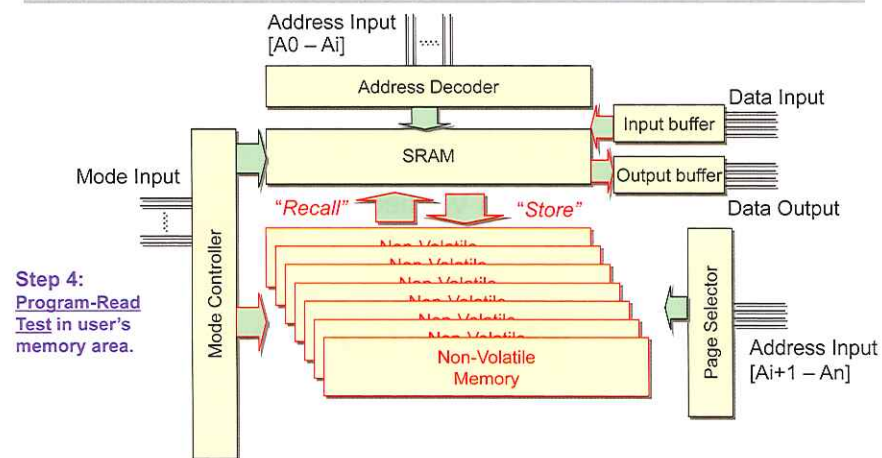


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Step 4 (after programming)

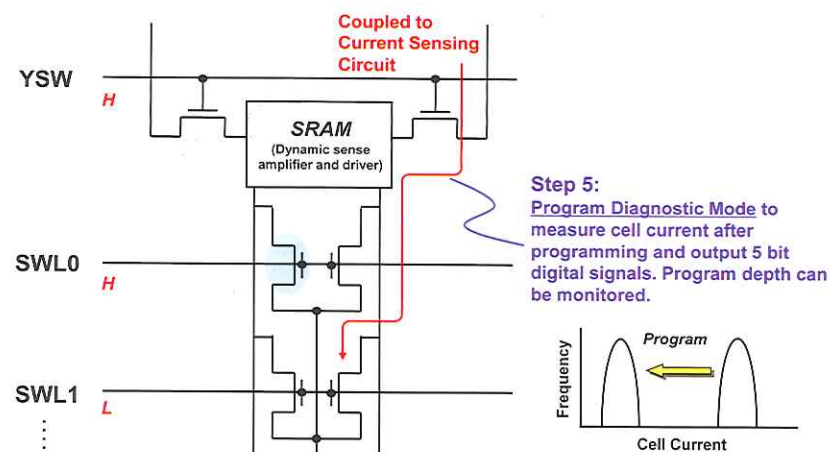


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Step 5 (after programming)



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OTP IP Lineup in TSMC Processes

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Availability in TSMC Processes

- ✓TSMC 0.18 μ m **IP9000 Full Qual.**, Volume Production
- ✓TSMC 0.13 μ m **IP9000 on-going**, Volume Production
- ✓TSMC 0.11 μ m Silicon Verified
- ✓TSMC 90nm Silicon Verified
- ✓TSMC 65nm **IP9000 Full Qual.**, Volume Production

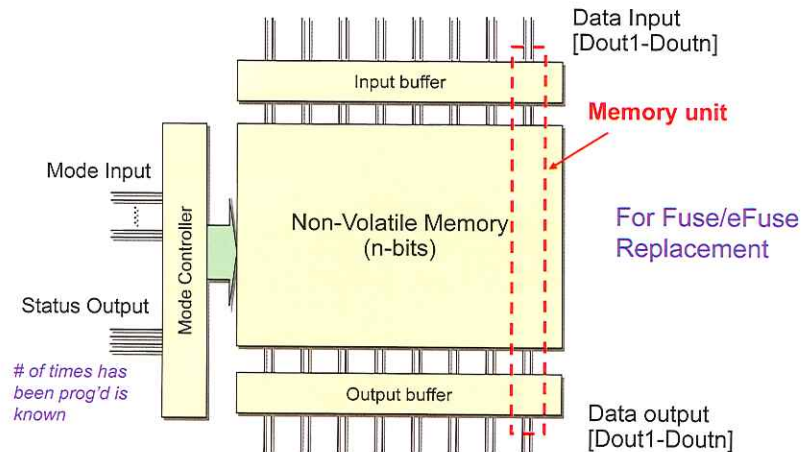


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Single-Word-Line Architecture for Small Memory Size



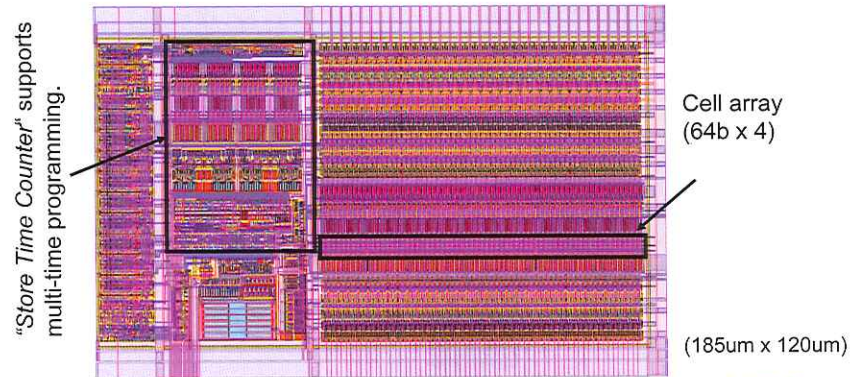
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256b OTP/64b 4-Time-Programmable

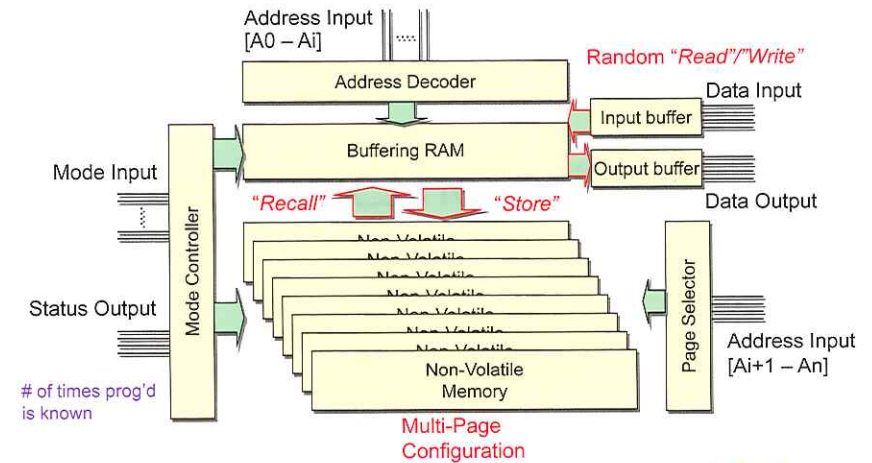
- Process Generation: 0.13 μ m Process
- I/O: 64b (configurable from 1b to 256b)
- Metal Usage: 3 Layers (no limitation on routing over the macro)



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SRAM-Like Architecture for Large Memory Size

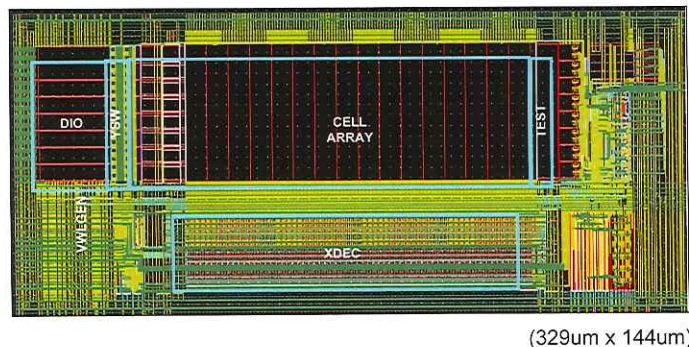


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16Kb OTP/4Kb 4-Time-Programmable

- Process Generation: 65nm Process
- I/O: 8b/16b/64b (pin option)
- Metal Usage: 3 Layers (no limitation on routing over the macro)



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OTP Memory Compiler

In 0.13 to 0.1 μ m generations, our OTP compiler supports the following variations of memory size from 4Kb to 320Kb and I/O pin count from 8 to 40.

		IO				
		8	16	24	32	40
		Column				
Row	64	4,096	8,192	12,288	16,384	20,480
	128	8,192	16,384	24,576	32,768	40,960
	192	12,288	24,576	36,864	49,152	61,440
	256	16,384	32,768	49,152	65,536	81,920
	320	20,480	40,960	61,440	81,920	102,400
	384	24,576	49,152	73,728	98,304	122,880
	448	28,672	57,344	86,016	114,688	143,360
	512	32,768	65,536	98,304	131,072	163,840
	576	36,864	73,728	110,592	147,456	184,320
	640	40,960	81,920	122,880	163,840	204,800
	704	45,056	90,112	135,168	180,224	225,280
	768	49,152	98,304	147,456	196,608	245,760
	832	53,248	106,496	159,744	212,992	266,240
	896	57,344	114,688	172,032	229,376	286,720
	960	61,440	122,880	184,320	245,760	307,200
	1024	65,536	131,072	196,608	262,144	327,680



320Kb OTP Layout in 0.13 μ m Process

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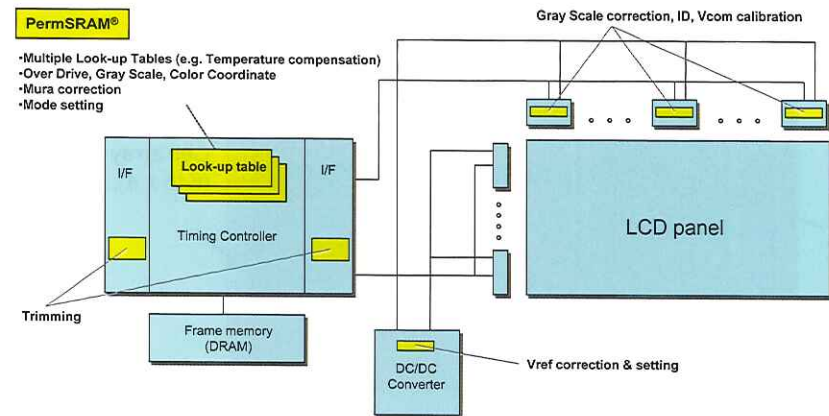
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Application Examples

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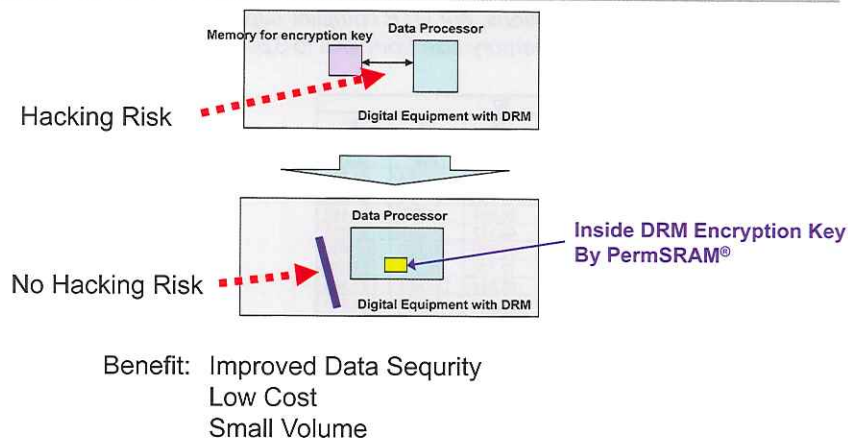
PermSRAM Applications (1)



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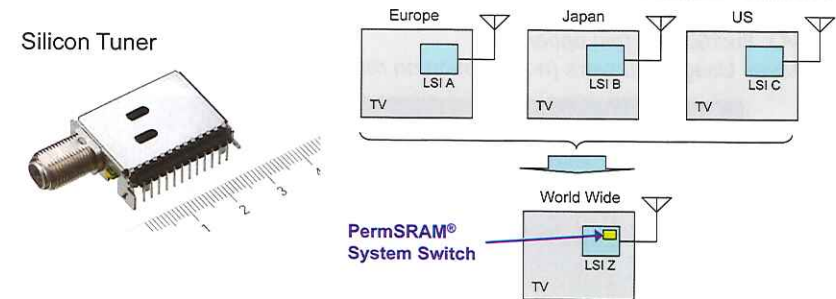
PermSRAM Applications (2)



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PermSRAM Applications (3)

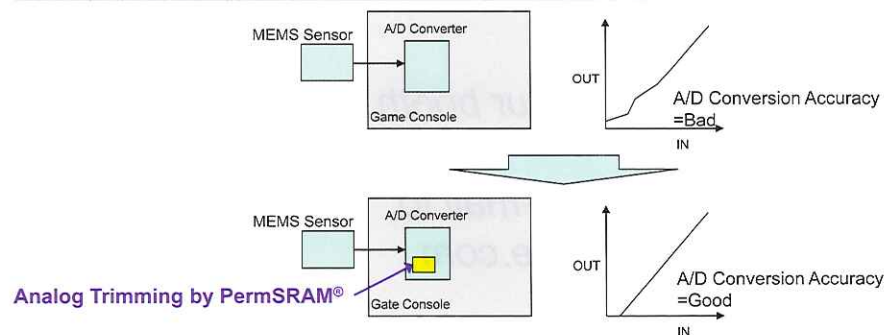


Benefit: Cost down for R&D
Cost down for Inventory Control
Cost down for Product Quality Control

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PermSRAM Applications (4)



Benefit: Small Volume
High Accuracy
Low Cost
Availability of Multiple Vendor Option for MEMS

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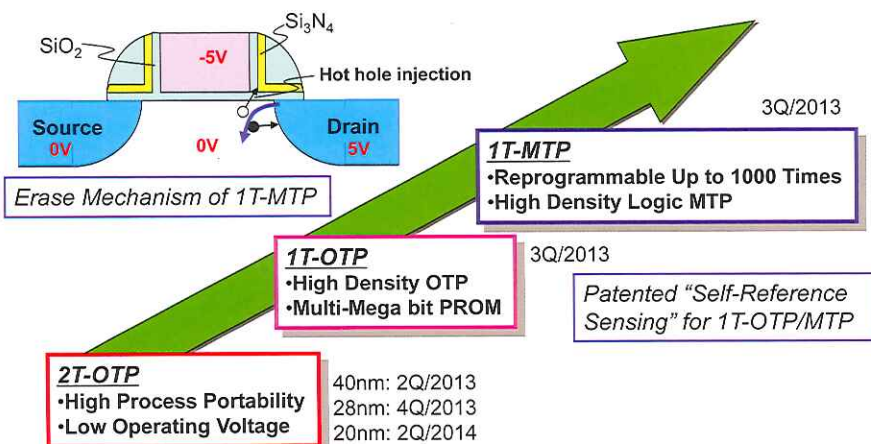
Roadmap

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NSCore's NVM Roadmap



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1T-MTP Key Features

- Available in Standard CMOS Process
- 1-Transistor Memory Cell
- Endurance: 1000 times
- Macro Area:
~0.2mm²/Mbit @ 65nm process node
~0.1mm²/Mbit @ 40nm process node

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Summary of Our Key Advantages

- *Field Programmable with Full Test Coverage*
- *High-Speed Programming at ~5.5V w/o Charge Pump*
- *Low-Voltage Operation down to 0.8V*
- *High Temperature Data Retention*
- *Invisible Memory Contents*
- *Wide Process Coverage from 180 to 65nm and Below in Standard Logic Processes*

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For more information

Please visit our booth #205.

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sales@nscore.com*

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NOTE

This image shows a single sheet of white paper with horizontal ruling lines. The lines are evenly spaced and run across the width of the page. There are no margins, text, or other markings on the paper.

TSMC 2012 Open Innovation Platform[®] Ecosystem Forum

The Trusted Technology and Capacity Provider



Advancing SoC Design and Analysis for Cloud-Connected Devices

Sonics

ABSTRACT

TSMC's advanced processes empower Moore's Law as SoC designers meet the challenge of the end-user experience for Cloud-scale SoCs used in cloud-connected devices. Critical to the user experience is achieving the right formula of performance with heterogeneous multicore designs leveraged by memory bandwidth and dramatically extending battery life. Since IP comes from many disparate sources, getting all the pieces integrated is an arduous and challenging element of the start up efforts for design managers. The SoC architecture is one of the earliest choices made in the SoC design cycle. This is frequently gated by integration of the various IP cores into a performance modeling environment such that key design trade-offs, including the number of CPU/GPU cores and basic system memory bandwidth requirements, can be resolved.

To speed the time from IP delivery to usable results, Sonics has worked with other key IP providers in pre-integration of various IP cores with Sonics' system IP, such that designers quickly and easily can drag and drop IP from Sonics' n-Core Integration Library. Using Sonics StudioXE, designers can quickly integrate pre-tested IP cores with Sonics' advanced on-chip networks. By In addition to a pre-tested socket protocol interface, end-to-end system analysis can also be achieved using data stimulus with Sonics' Performance Analysis tools. With Sonics' n-Core Integration Library, users can rapidly create their SoC architecture with performance modeling software and stimulus all set up.

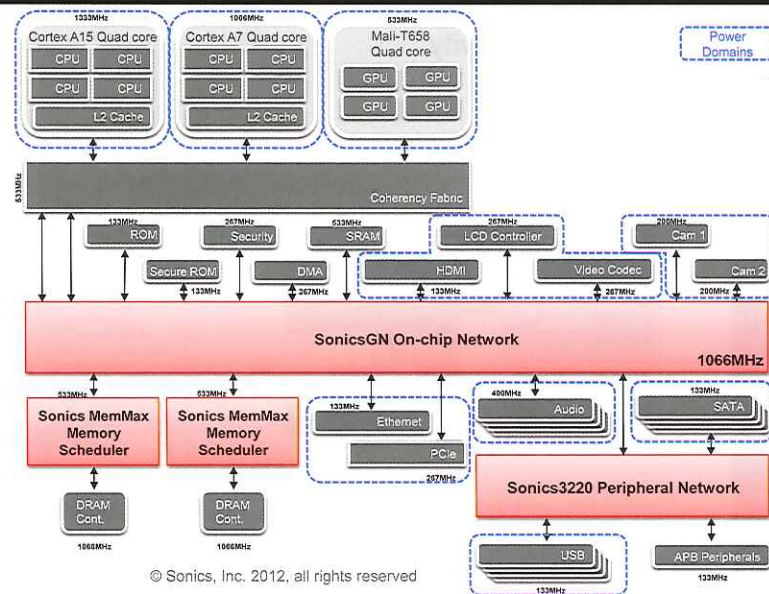
Different views and scenarios supported by this environment will also be explored and reviewed during the demonstration.



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Example Tablet Application Processor



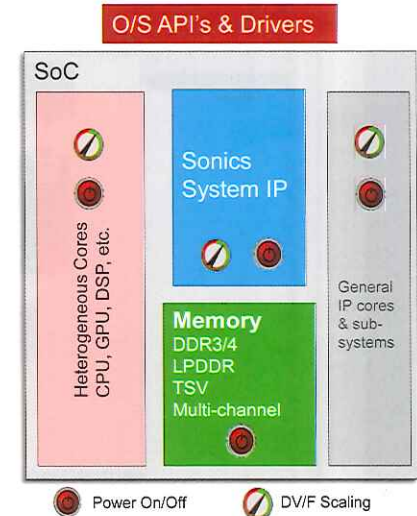
5

Sonics, the System IP Leader



■ We provide the IP, technology, and tools used to architect SoCs

- Interconnect
 - Coherency
- Memory Subsystems
- Power Management
- Security
- Performance IP & Analysis



6

Designer Challenge

Complete SoC Realization Support



- **SoC Architect**
 - Early stage architectural exploration
- **Front-end team**
 - Support multiple interface protocols/widths
 - Performance/power/area optimization
 - Include last minute changes in requirements
 - Large amount of functional verification
- **Backend team**
 - Design topology could complicate timing closure
 - Many iterations on P&R for critical timing path resolution
- **CAD team**
 - Integrate different 3rd party IP/tools into the SoC development environment

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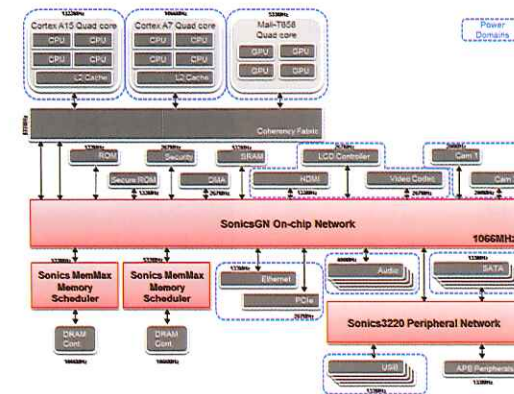
7

Architectural Exploration



SoC Architects' Challenge

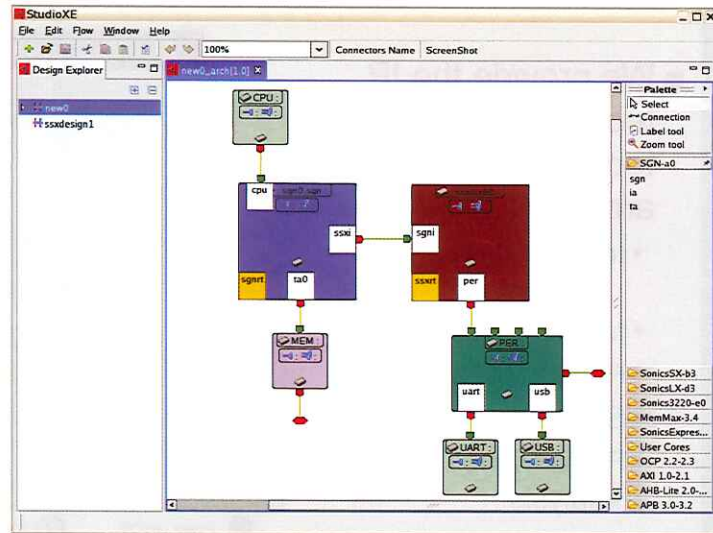
Explore behavior of complex SoC prior to integration



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Block Editor View



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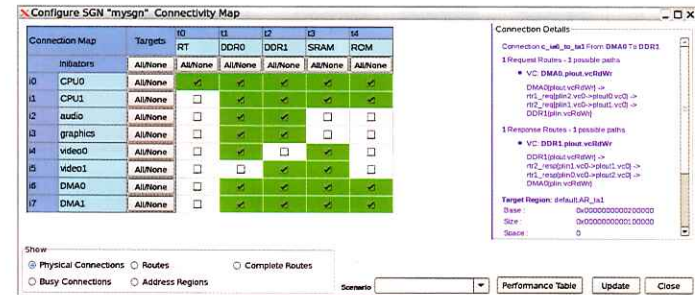
Connectivity Map



■ Define connectivity

■ Review overlay

- Physical connections
- Routes
- Traffic per scenario
- Address map



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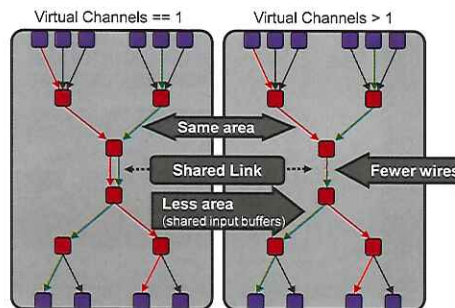
Concurrency – How it works



■ SGN performance features

- Virtual Channels (VCs)
- Split Transactions
- Pipelined Paths
- Multiple Outstanding Transactions
- Non-blocking flow control
- QoS

VCs allow system resources to be maximized for greater network efficiency



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Concurrency – Optimize the Network



■ Blocking networks cannot avoid periods of 0 progress

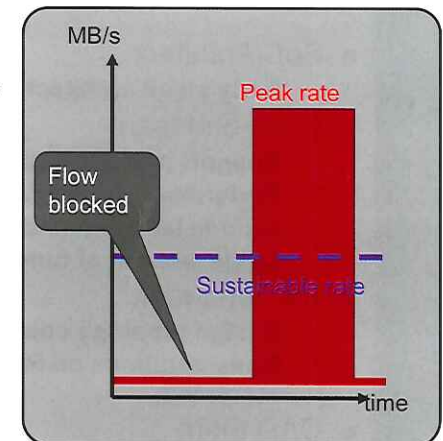
- Peak rate MUST be raised to maintain a sustainable rate
- IP core buffering needed at edge of the network

■ Non-blocking network

- Higher network efficiency
- Lower peak rate for same sustainable rate

■ Non-blocking multi-threading networks advantages

- Less jitter in rate, smaller buffers, shorter power down



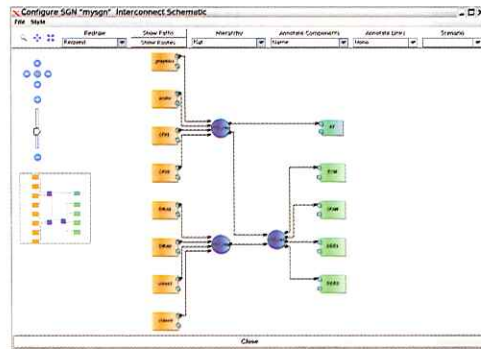
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Network Configuration



- Build/modify topology
 - Auto-draw
 - Context sensitive with error checking
- Views
 - Power & Management domains
 - REQ and/or RSP
- Annotated
- Paths displayed



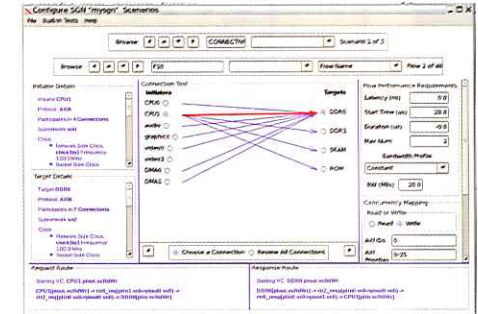
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Scenario Capture



- End-to-end traffic flow
 - BW Profiles: Constant, normally distributed, exponential, bursty, ...
 - Mapped to one and only one Connection
 - Bandwidth requirements
 - Optionally: Burst size constraints, addressing ranges, QoS inputs
- Multiple traffic flows collected into mode-specific scenarios
 - For simulation
 - Design constraints



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Performance Analysis (VSPA)



- Dynamic performance analysis
- Based on traces
 - Captured from System C simulation
 - Auto-generated test bench
 - Auto-generated and/or user-crafted stimulus

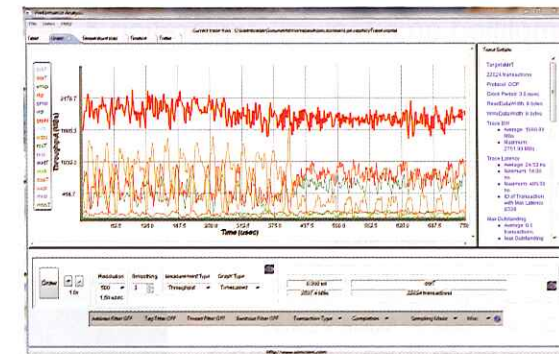
Visual & interactive

- | | | |
|---|--|--|
| <ul style="list-style-type: none"> ■ Views <ul style="list-style-type: none"> • Tabular • Trellis • Graph • Temperature Map • Timeline | <ul style="list-style-type: none"> ■ Measurements <ul style="list-style-type: none"> • Throughput • Latency • Outstanding • Rate | <ul style="list-style-type: none"> ■ Style <ul style="list-style-type: none"> • Time-based • Histogram • Cumulative Histogram |
|---|--|--|

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Performance Analysis (VSPA)

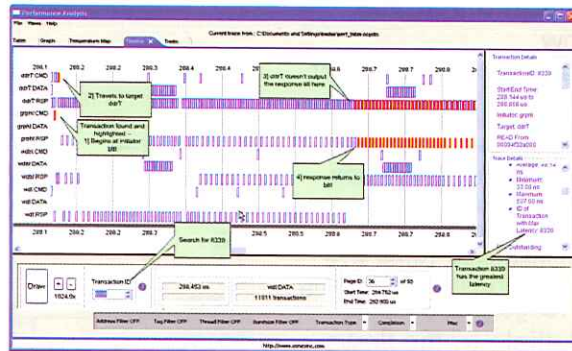


- | | | |
|---|--|--|
| <ul style="list-style-type: none"> ■ Views <ul style="list-style-type: none"> • Tabular • Trellis • Graph • Temperature Map • Timeline | <ul style="list-style-type: none"> ■ Measurements <ul style="list-style-type: none"> • Throughput • Latency • Outstanding • Rate | <ul style="list-style-type: none"> ■ Style <ul style="list-style-type: none"> • Time-based • Histogram • Cumulative Histogram |
|---|--|--|

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Performance Analysis (VSPA)



Views

- Tabular
- Trellis
- Graph
- Temperature Map
- **Timeline**

Measurements

- Throughput
- Latency
- Outstanding
- Rate

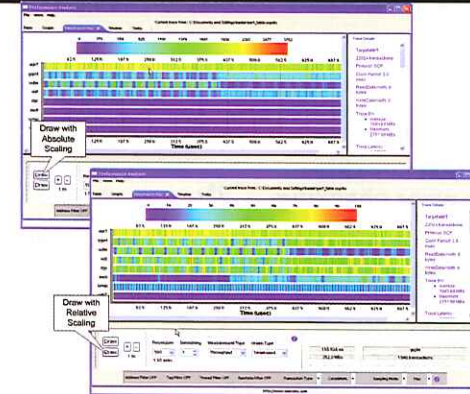
Style

- Time-based
- Histogram
- Cumulative Histogram

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Performance Analysis (VSPA)



Views

- Tabular
- Trellis
- Graph
- **Temperature Map**
- Timeline

Measurements

- Throughput
- Latency
- Outstanding
- Rate

Style

- Time-based
- Histogram
- Cumulative Histogram

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SonicsStudioXE™ Development Environment



Simplified architectural exploration & behavioral modeling

- Behavioral models (QuickCore Models)
- Stimulus generation (Socket Transaction Language or Verilog Tasks)
- Analysis capabilities (Runtime & Post Simulation Analysis Tools)

Automated configuration and integration

- Capture -- SOC design, synthesis constraints
- Generation -- RTL, SystemC, synthesis scripts and testbench
- Estimation -- Area, Speed

Performance modeling

- SystemC simulation
- Quick Models for masters/slaves

Interface to third-party tools

- Simulation (MTI/NCVerilog/VCS)
- Synthesis (DC/RC)
- Power (CPF)



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Automated Verification and Traffic Generation



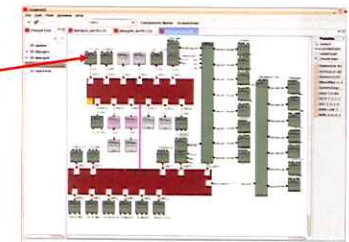
Test suite*

- Automatically generate functional testbench for user-specific design configuration
- Includes functional testing and code coverage

Smoke Test

- Automatically generate simple SmokeTest stimulus by utilizing Socket Transaction Language (STL)
- Feed STL to SonicsQuick Models for simulation

```
version 2.0
#initiator ia_CPUX_ia to target ta_SRAM
100 : writenonpost 0x40020000 0x6d
110 : writenonpost 0x4003FF00 0x6e
120 : read 0x40020000
130 : read 0x4003FF00
#initiator ia_CPUX_ia to target ta_DSP
140 : writenonpost 0x50000000 0x8c
150 : writenonpost 0x53FFFF00 0x96
160 : read 0x50000000
170 : read 0x53FFFF00
```



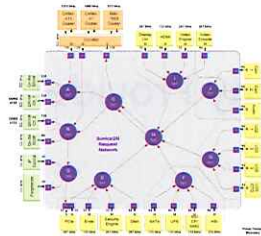
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Sonics Delivers GHz+ Performance



- **SonicsGN achieves > 1GHz**
 - Supports A15/A7 based tablets
 - TSMC 28nm HPM Standard VT
- **Active Power: 1μW per MByte of bandwidth**
- **Optimized for SoC environment**
 - Input-buffered routers
 - Distance spanning links
 - Credit-based flow control
- **Architect's plan implemented through backend**
 - Virtual channels enable non-blocking network
 - Quality of Service
 - Security
 - Error management



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Summary



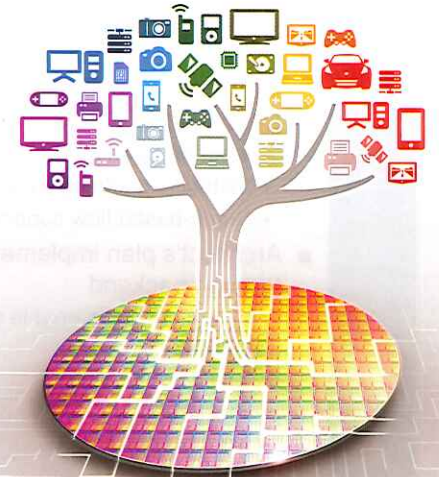
- GHz, GFLOPs and GB/sec. are today's consumer design points
- SoC integration must **exploit** that performance
 - Memory bandwidth – optimized multichannel scheduling
- ... while **improving** battery life
 - Automatic hardware power management, with software policies
- **Cloud-Scale SoC's require room to grow...**
 - **Twice** the frequency
 - **One half** the SoC power
 - **Scalable** range of solutions

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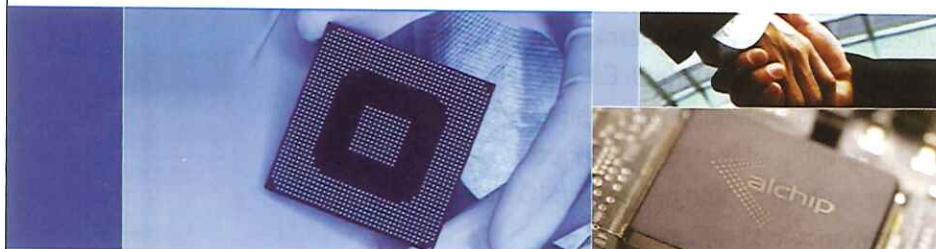
65GP Area-I/O Chip Design Alchip



ABSTRACT

Due to high I/O pin count, adoption of flip-chip and area-I/O technology provides better cost and performance advantage. In this article, we present a TSMC 65GP networking design in which four DDR3-1066 macros were implemented. Each macro had controller and PHY connected to 350 custom IO pads. The peripheral-I/O design made DDR3 macro 15000um wide, which seriously impacted chip-level floorplan and failed performance target. With the adoption of Area-I/O, the width of macro was controlled to be 3000um and performance target was met. The clear guideline from TSMC facilitated design verification and made Area-I/O free of ESD risk. The silicon result proved that Area-I/O design on 65GP process led to robust performance and reliability.





65GP Area-I/O Chip Design

Trusted Silicon Partner Realizing Innovations

Contents



- Flip-chip and Area-I/O concepts
- Area-I/O chip overview
- Area-I/O alignment strategy
- ESD verification
- RDL (Re-Distribution Layer) design
- Conclusion

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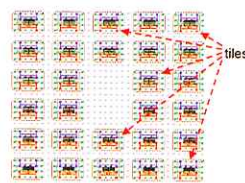
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2

Flip-chip and Area-I/O Concepts



- Flip-chip
 - Direct connect between die and substrate, eliminating bond wires inductance and capacitance
 - Better heat dissipation through bumps
- Area-I/O
 - I/O cells placed anywhere on a chip
 - Shortest I/O-to-ball wiring length
 - I/O cells not restricted to peripheral region
 - Highest possible pin count



Data source:
TSMC area-I/O design guideline

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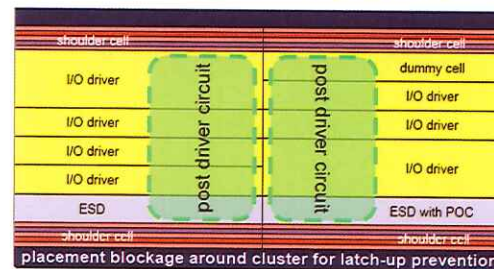
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3

Cluster I/O Concepts



- I/O cells in clusters facilitate power/ground connection
- Back-to-back I/O cells always place post-driver circuits at center of the cluster
 - Blockage for latch-up prevention around I/O cells is reduced



Data source: TSMC area-I/O design guideline

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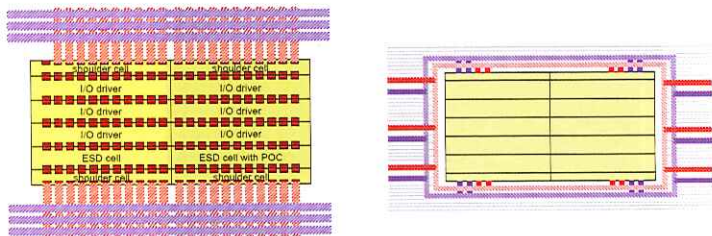
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4

Power Planning Guidelines



- Power connection through shoulder cells
- Core VDD/VSS rings created around clusters
- Clusters may share the same power mesh

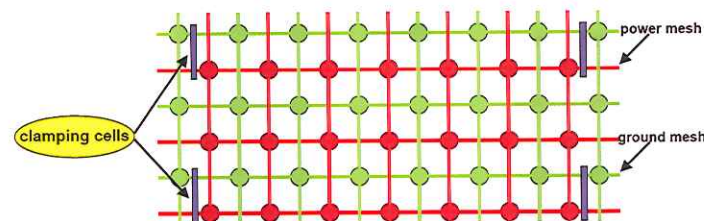


Data source: TSMC area-I/O design guideline

Core ESD Protection Guidelines

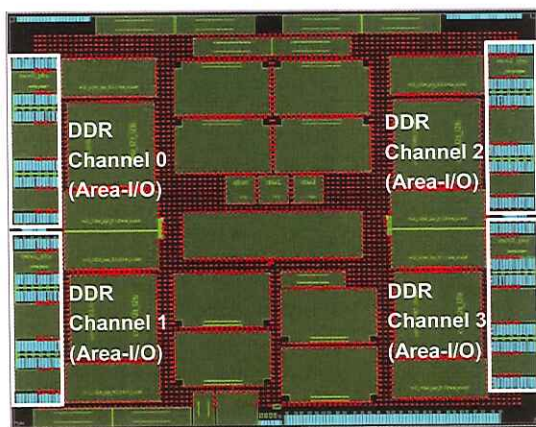


- Adequate ESD clamp cells placed evenly in each power domain
- Clamp cells placed as close to bumps as possible



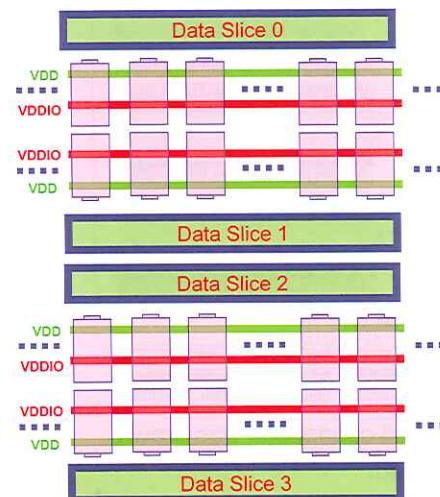
Data source: TSMC area-I/O design guideline

Area I/O Chip Overview



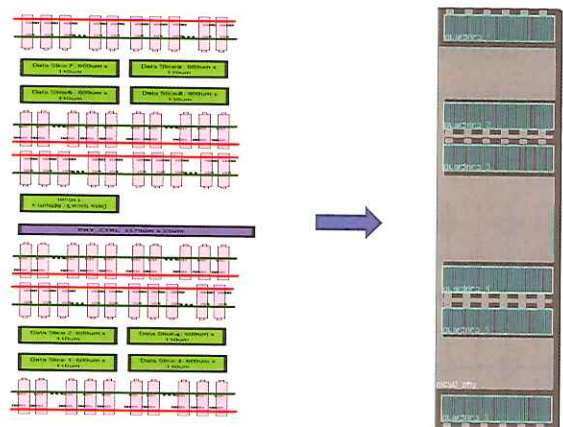
- TSMC 65nmGP, 1P8M+RDL
- HFCBGA, 1517 balls
- Die size
 - 20.6mm * 17mm
 - Approx. 60M gates
- 4-channel DDR3 I/F
 - 72-bit per channel
 - Area-I/O adopted in DDR PHY

DDR3 I/O Cluster Design



- Created DDR3 I/O clusters following TSMC area-I/O guideline
- I/O cells are back-to-back with post-driver power rail (VDDIO) at center of cluster
- DDRs data slices placed between I/O clusters

Area-I/O Alignment Inside 9-lane DDR PHY (72-bits)



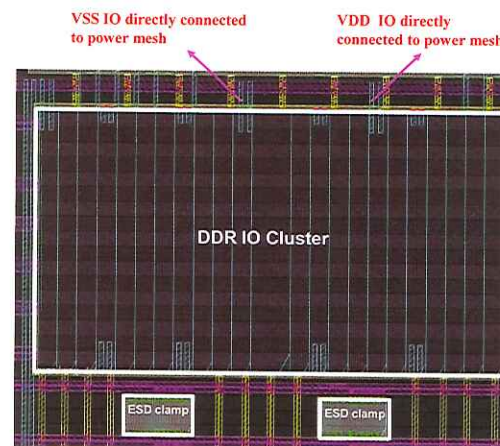
Conceptual Area-I/O design of a 9-lane DDR3 PHY

Actual layout implementation

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ESD Clamp and Power Connection

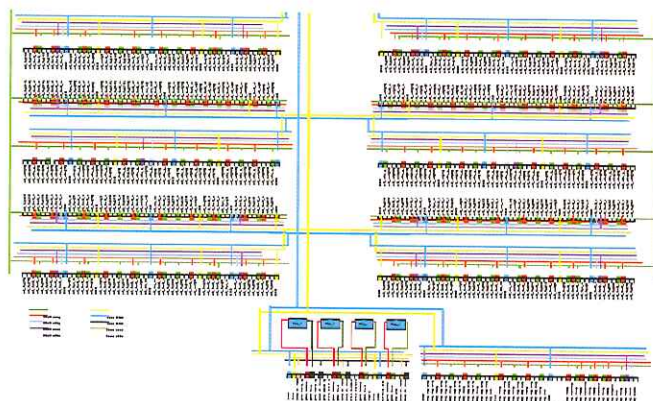


Except ESD clamps in I/O cluster, additional ESD clamp cells were added around I/O cluster to enhance ESD performance

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ESD Verification

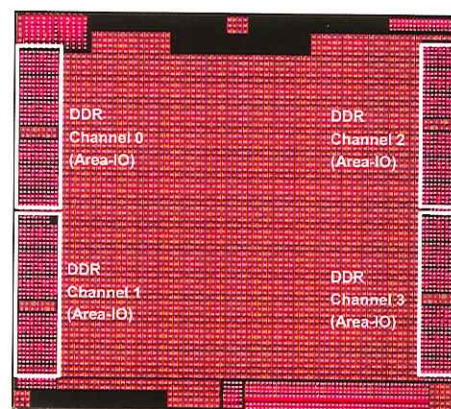


- Diagram of power/ground rail connection was drawn
- Discharge paths were verified
- Resistance values were calculated

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RDL and Bump Design Overview



- Bump and RDL sub-modules were created
- Distance between area-I/O cells to corresponding bumps was well balanced

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Conclusion



- Following TSMC area-I/O design guidelines, a large networking SoC was designed with 65nmGP process
- Area-I/O reduced area 30% compared to peripheral I/O designs
- Silicon result showed that performance, reliability and ESD robustness of DDR I/O all met design target



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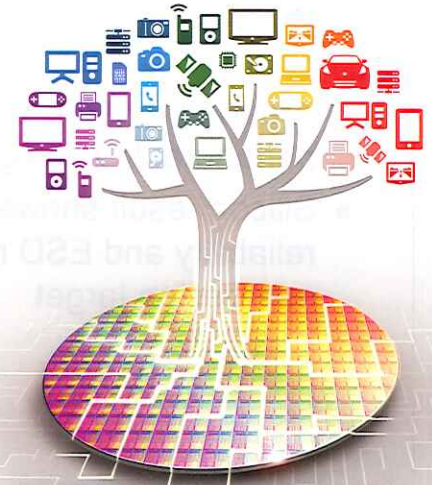
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Case Studies for Multi-Standard High Performance and High Portability SerDes IP Design

GUC

ABSTRACT

To adapt to highly dynamic and demanding customer IP customization needs, GUC's IP team has developed high portability design methodologies. In this presentation, GUC's 10G KR IP will be used as a case study.

GUC's 10G KR PHY possess the following advantages for high performance and high portability:

- (1) Hybrid analog/digital architecture offers low power, compact area, and flexible configuration.
- (2) Easy porting due to RTL based CDR/SIPO/PISO, etc.
- (3) Designed for harsh SoC environments.
- (4) Built-in programmable transmit and receive equalization for optimized signal integrity
- (5) Embedded BIST function as well as RX internal eye monitoring for high volume production and low cost test.
- (6) Comprehensive Chip-Package-Board design flow guarantees first silicon function and performance

GUC has successfully migrated 40nm 10G KR IP to 28HPM and taped out in Q2 2012.





Case Studies for Multi-Standard High Performance and High Portability SerDes IP Design

Jen-Tai Hsu, Ph.D., Tony Chen

GUC's Multi-Standard KR SerDes

Standard	Data Rate (Gb/s)	40nm	28nm
GigE, XAUI	1.25, 3.125	Available	Available
RXAUI	6.25	Available	Available
XFI/SFI	10.3125	Available	Available
10GBase-KR	10.3125	Available	Available
CEI-11G	11.1	Available	Available
PCIE I/II/III	2.5, 5.0, 8.0	-	Available soon
SATA I/II/III	1.5, 3.0, 6.0	-	Available soon
SAS I/II/III	3.0, 6.0, 12.0	-	Available soon

P2

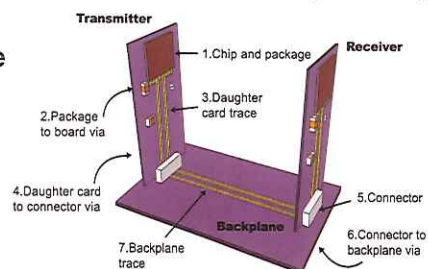
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Uncompromising Performance

GUC Multi-Standard KR SerDes IP Highlights

- 1.25Gb/s to 12.5 Gb/s data rate
- Multiple standard support for telecom, computing, and storage applications
- Supports IEEE 10GBase-KR (802.3AP) over 40" of backplane
- Excellent TX and RX performance
- Adaptive TX and RX equalization for optimized signal integrity
- On-die eye monitor
- Extensive BIST coverage



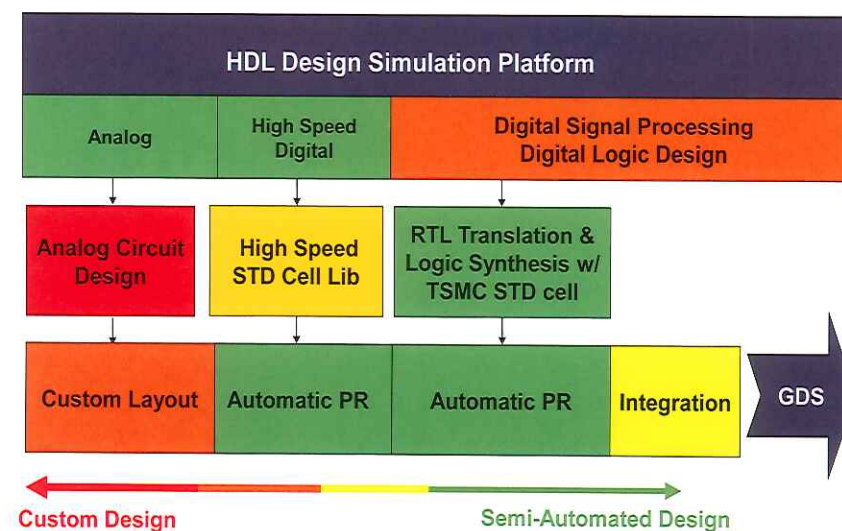
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High Portability Design Flow



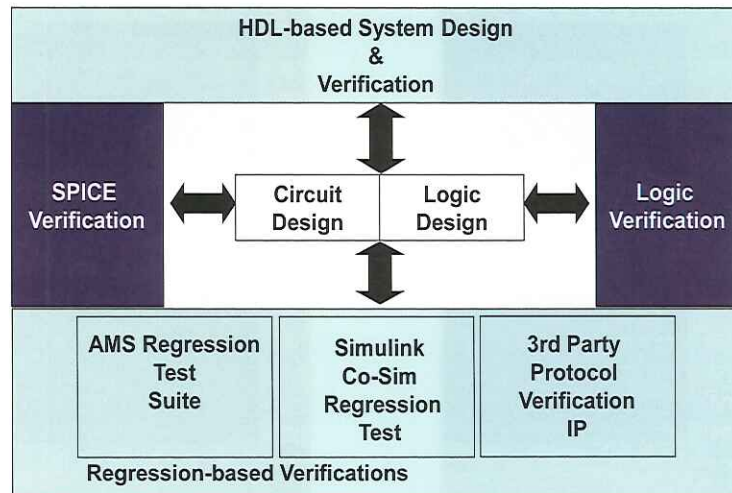
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High Portability Design Flow



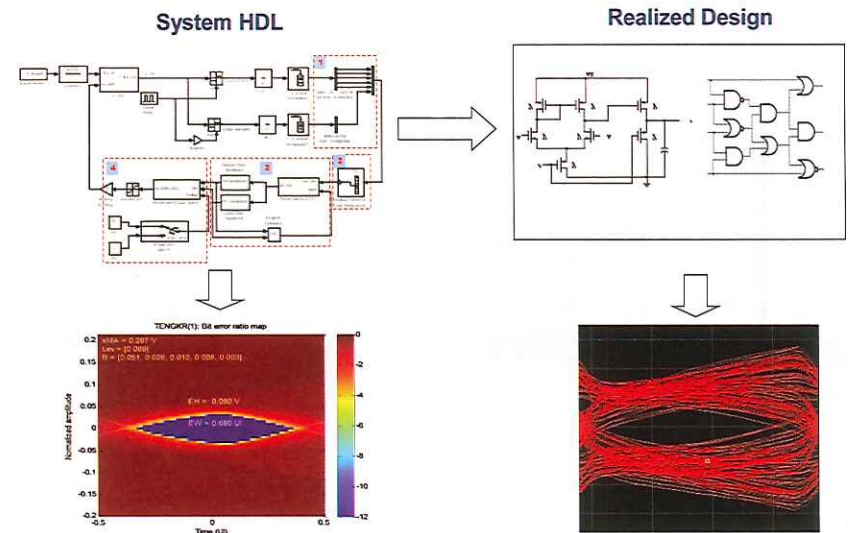
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High Portability Design Flow



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High Portability Design Flow

- Highly scalable and highly structured SerDes architecture
- HDL driven top-down design and bottom-up implementation
- Scalable and programmable analog circuits
- High speed custom STD cell library supports high speed APR flow
- Widely adopted digital signal processing and standard logic design flow
- Rigorous verification and regression testing at block and system level

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Multi-Standard KR SerDes: An Overview

Process	TSMC 40nm	TSMC 28nm
Supply Voltage	0.9V Core 1.8V I/O	0.9V Core 1.8V I/O
Metallization	7M+ (5X1Z) minimum	7M+ (5X1Z) minimum
Package	FC-BGA	FC-BGA
Number of Lanes	4	4
Power Dissipation / Lanes	180mW (KR) 160mW (Non-KR)	120mW (KR) 100mW (Non-KR)
Area	2.1mm ² (4-lane PHY)	1.45mm ² (4-lane PHY)

P8

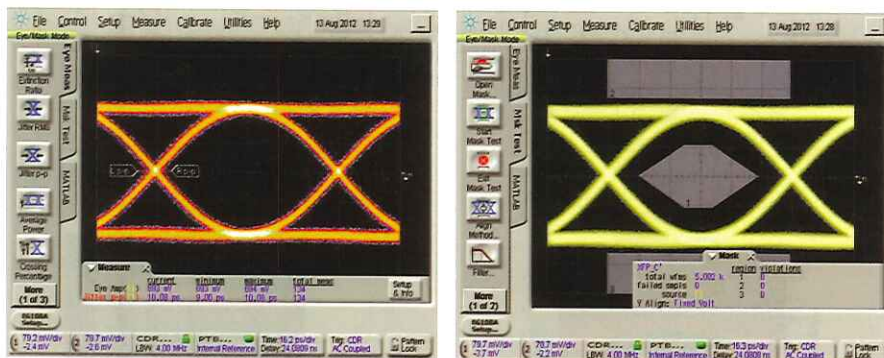
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Key Characterization Data: TX

Extremely clean PRBS31 eye diagrams @ 10.3125 Gb/s



P9

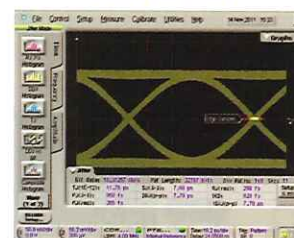
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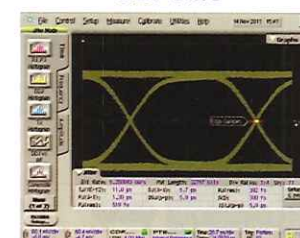
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Key Char Data: TX Jitter at Different Data Rates

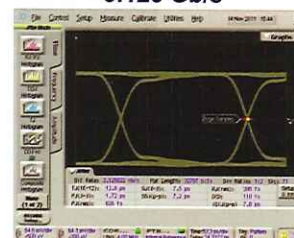
10.3125 Gb/s



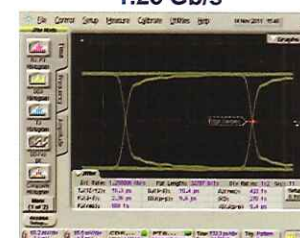
6.25 Gb/s



3.125 Gb/s



1.25 Gb/s



P10

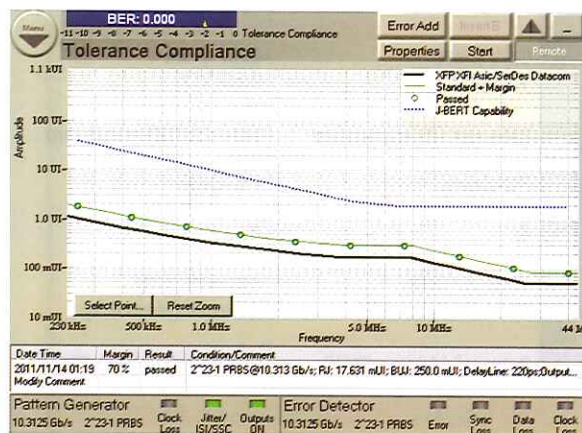
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Key Char Data: RX Jitter Tolerance

XFI Jitter Tolerance with excellent margin



Added:
0.2UI DJ
0.2UI RJ
0.25UI BUJ
+ SJ

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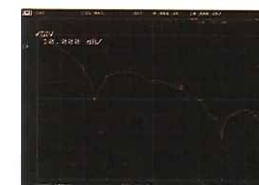
Key Char Data: Backplane Performance



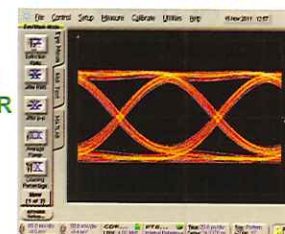
40" backplane



Severely Distorted Signal!



Equalized & Recovered Data

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10G KR

P12

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Deliverables

- **Datasheet**
- **Behavioral verilog model**
- **LEF**
- **Layout GDS file**

P13

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Implementation of ARM Cortex-A9 Quad Core Processor with Synopsys Hierarchical Flow Open-Silicon



ABSTRACT

The design involves four CortexA9 cores (quad core) and L2 Cache controller with 512KB of L2 cache memories. There were multiple challenges in the implementation since we have restrictions on the I/O placement and the shape of the block at the SOC level. The timing constraints for single core were derived with respect to the top level implementation using ICC budgeting flow. This quad core implementation has to meet the performance goals with a specific area and leakage power targets.

The block implementation is done in a hierarchical fashion using tools suite from Synopsys. The single core (falcon_cpu) is synthesized with DC-T SPG flow using the same floor plan information used for the physical implementation with IC-Compiler.

Synthesis and physical implementation of the single core is done with low-Vt cells to get the best performance possible. Various optimization techniques in Synopsys IC-Compiler were used, to get the frequency goals for the single core which includes skewing the clock of some of the registers and integrated clock gating cells, path group weights, applying net weights for clock gating outputs, etc. Leakage optimization is done using efficient leakage optimization techniques from IC-compiler at the end of the implementation without degrading timing performance.

Multiple floorplan iterations were done in IC-Compiler at the quad core level to optimize the L2 cache memory placement and L2 cache controller logic. Since the L2-cache memory instance sizes are fairly big, the main challenge at the quad core level was to get the optimal placement for the memory hard macros and the different logic modules without increasing the area. Features like move (fixed) bounds, floating bounds and partial/buffer only blockages in ICCompiler were used to get the optimal placement of the top level modules.

Eventually this effort resulted in meeting the performance, power and area targets set for the design.



Implementation of ARM Cortex-A9 Quad Core Processor with Synopsys Hierarchical Flow

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Outline:

- ❖ Design details and challenges
- ❖ Falcon core implementation
- ❖ Quad core top implementation
- ❖ Results and summary

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Design Details

- ❖ ARM Cortex-A9 Quad Core processor
 - Each core with Neon with VFP, 32KB L1 cache and 128bit TLB, SCU
- ❖ L2 Cache Controller and Cache Memories
 - 512KB L2 cache memories, PL310 controller
- ❖ TSMC 40nm LP Process with multi channel LVT libraries (C40 & C50) and 8M (5x2z) metal stack
- ❖ 3.1 Million standard cell Instances and 216 macros

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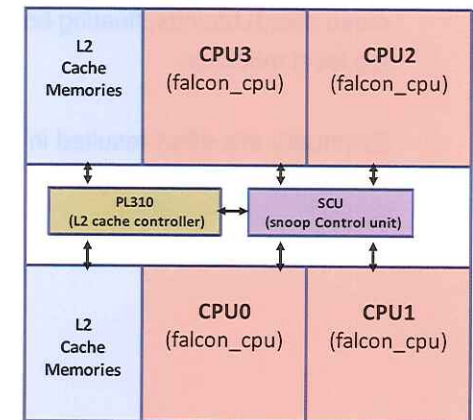
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Quad Core Implementation Overview

- ❖ L1 cache, neon, d-side and i-side logic are part of falcon_cpu core
- ❖ L2 Cache, Cache controller and SCU are part of the quad core top level
- ❖ Falcon_cpu core is implemented once and instantiated 4 times
- ❖ Complete implementation is done with C40 libraries and leakage recovery is done post route SI optimization

Quad Core Top Block Diagram



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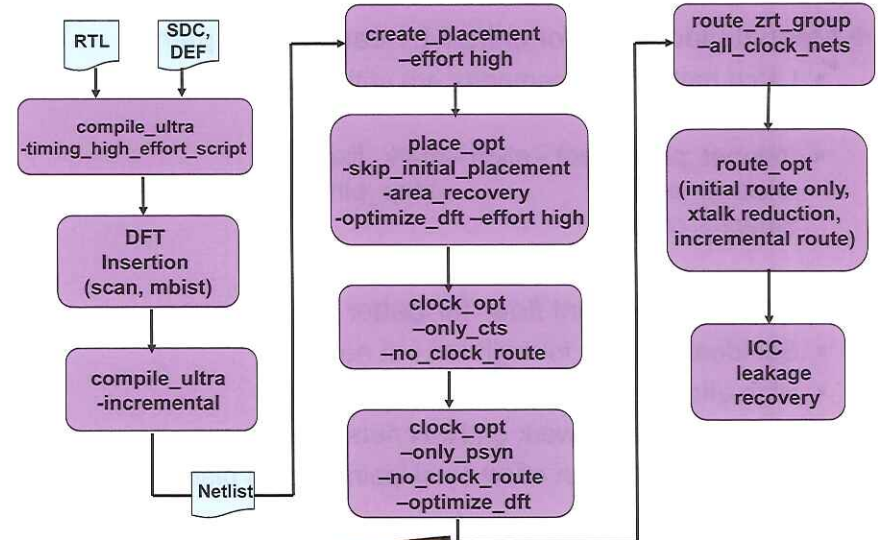
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Design Challenges

- ❖ CPU timing is very sensitive to the cell placement and required good correlation between synthesis and physical implementation
- ❖ Quad Core floorplan with best possible placement for SCU tag memories, L2 cache memories and Cache controller with best possible area
- ❖ Leakage power reduction without impacting the performance

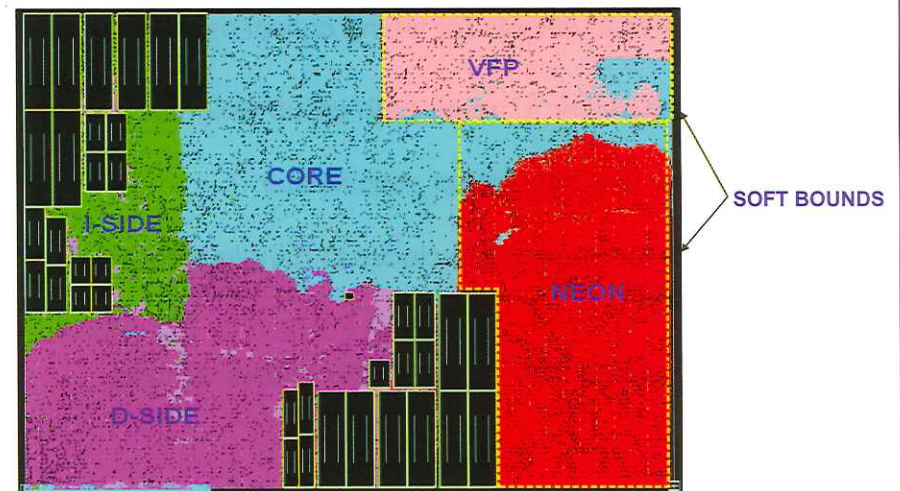
Falcon_cpu Flow Diagram



Falcon_cpu implementation - Synthesis

- ❖ High effort DCT synthesis with compile_ultra command
- ❖ Model clock skew for ICG pins for better data path optimization
 - set_clock_latency 0.8 \${icg_clkin_pins}
 - set_clock_latency 1.0 \${icg_clkout_pins}
- ❖ Multiple Path Groups with weights for timing critical modules
 - dside, core, neon and L1 cache read/write paths

Falcon_cpu implementation - Floorplan



Falcon_cpu implementation - Placement

- ❖ Magnet placement for critical L1-cache RAM paths
 - Latch paths from memories are critical and needs the magnet placement
 - magnet_placement -align -mark_fixed -exclude_buffers -stop_pins [\$latch_pins] [get_cells \$macro_cells]
- ❖ Two Pass placement flow for better performance
 - Set ideal network for high fan out nets
 - High effort timing driven global placement
 - Remove ideal network on HFN nets
 - place_opt with high effort by skipping global placement

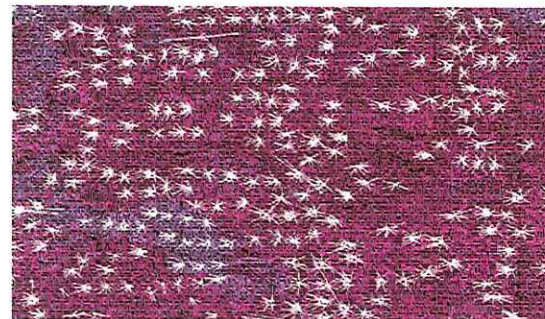
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Falcon_cpu implementation – ICG Placement

- ❖ ICG placement and optimization:
 - Enable auto bounds with area multiplier for gated registers
 - set placer_disable_auto_bound_for_gated_clock false
 - set placer_gated_register_area_multiplier 2
 - Apply high net weights on ICG output clock nets



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Falcon_cpu implementation - Placement & CTS

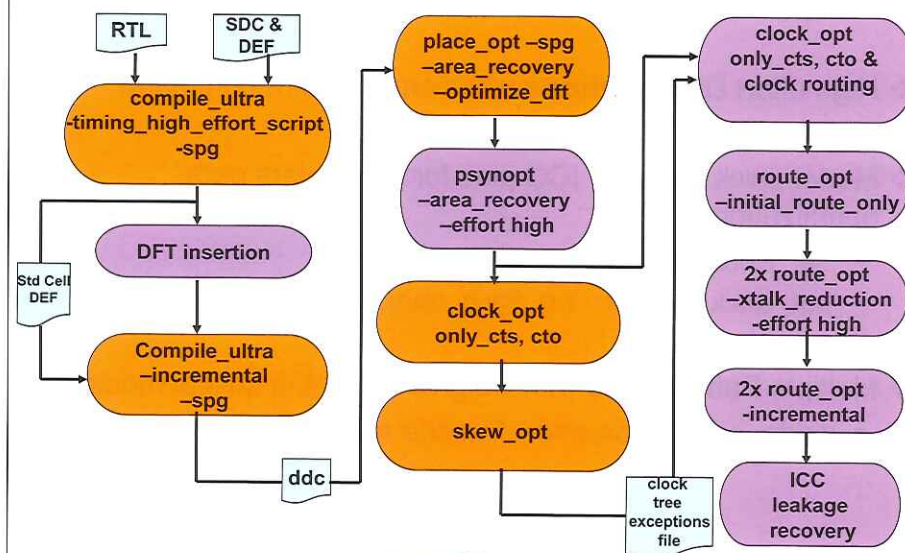
- ❖ Path groups with weights for timing critical modules
- ❖ Making detail placer to honor path group weights during legalization
 - set placer_use_path_group_weights true
- ❖ Useful skew for L1 memory clocks to handle memory write half-cycle paths
- ❖ Clocks are routed with double width and 4x spacing

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Cortex-A9 Quad Core Flow Diagram



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Quad Core Top implementation - Synthesis

- ❖ DCT SPG flow for better timing correlation between synthesis and ICC physical implementation
- ❖ Path groups with weights for ICG enables, SCU and L2 Cache controller modules
- ❖ Ungroup the combinational logic for better timing optimization
 - `set ungroup [get_designs * -f "is_combinational == true"]`
- ❖ Model skew for ICG Clock pins for better data path optimization

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Quad Core Top implementation - Placement

- ❖ Falcon_cpu single core implemented once and instantiated 4 times at quad core level.
- ❖ Floating move bounds for scu and pl310 modules and hard move bound for Interrupt controller
- ❖ Quad core top level utilization is low, with max cell density threshold setting cell placement and hence timing is improved
 - `set placer_max_cell_density_threshold 0.7`

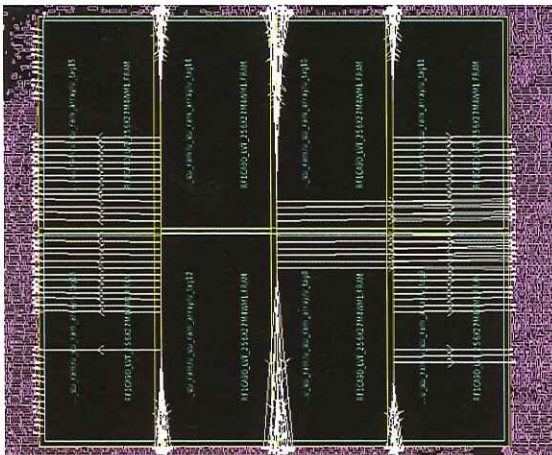
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Quad Core Top implementation - Placement

- ❖ Magnet placement for SCU memory read latches



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Quad Core Top implementation – CTS

- ❖ Falcon_cpu ILM models are used to build quad core clock trees
- ❖ skew_opt for few path groups to improve timing and find it very helpful for ICG paths
 - `skew_opt -path_groups {.....}`
- ❖ CPU clock is built first followed by other functional and DFT clocks
- ❖ Four cores are balanced differently based on the timing slacks for each core

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Quad Core Top implementation - Routing

- ❖ Clock are routed with double width and 4x spacing
- ❖ Post route optimization:
 - ❖ 2x route_opt -xtalk_reduction (SI, area and timing)
 - ❖ 2x route_opt -incremental (drc fixing)
- ❖ Leakage optimization is done post route with LVT long channel libraries
 - Use "focal_opt -power" for foot print compatible cell swapping

Static Timing Analysis Flow

- ▶ RC parasitic extraction is done with Star-rcxt tool.
- ▶ SI aware timing analysis is done with PrimeTime-SI tool for multiple modes and corners.
- ▶ OCV derate of 8% is applied to clock for setup analysis and 10% for hold timing analysis.
- ▶ Clock uncertainty is 50ps for both setup and hold timing analysis for sign-off.
- ▶ Timing ECO's are generated from PT-SI for timing closure.

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Results: falcon_cpu

- ❖ Total Instance Count: 645K
- ❖ Area and Utilization: 2.8 mm² & 85%
- ❖ Timing derate :
 - 8% early - setup
 - 10% late - hold
- ❖ CPU Performance

Corner	Process	Voltage	Temperature	Frequency
Cworst	SS	0.99v	125C	845 MHz
Cworst	SS	1.08V	125C	960 MHz
Typical	TT	1.1V	25C	1.27 GHz

Results: Quad Core

- ❖ Total Instance Count:
 - 3.1 million (includes 4 cores)
 - 520K (excludes 4 cores)
- ❖ Area and Utilization: 18.9 mm² & 59%
- ❖ Timing derate :
 - 8% early - setup
 - 10% late - hold
- ❖ Performance :

Corner	Process	Voltage	Temperature	Frequency
Cworst	SS	0.99v	125C	815 MHz
Cworst	SS	1.08V	125C	920 MHz
Typical	TT	1.1V	25C	1.2 GHz

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Results: Quad Core

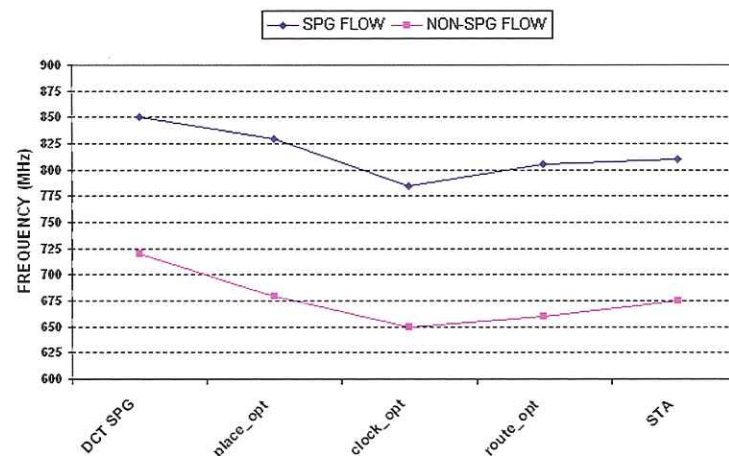
- ❖ Vt distribution after leakage optimization:
 - LVT C50 : 69% (2.15 Million)
 - LVT C40 : 31% (950K)
- ❖ Leakage Power (@ ffg, 1.21v, 125c)
 - Falcon_cpu: 220mW
 - Quad core : 2.1W (including 4 cores)
: 1.22W (excluding 4 cores)

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Results: Quad Core Performance



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Summary

- ❖ Two pass placement flow for falcon_cpu core
- ❖ SPG flow is extremely useful to improve the QOR and run times for quad core design
- ❖ Path groups with weights for critical modules and ICG enable paths
- ❖ Magnet placement for L1 cache and SCU memory read paths
- ❖ Leakage power recovery only after routing with focal_opt

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ACKNOWLEDMENT:

- ❖ Harissh Swaminathan – Synopsys, India
- ❖ Shrikrishna Mehetre – Open-Silicon, India

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Combining Design and IP to Deliver a Low Power / Low Cost 10GbE Controller

Uniquify

ABSTRACT

In this presentation we discuss the design and implementation of a new generation of low-power, low-cost 10 Gigabit Ethernet Controllers for Tehuti Networks that are being fabricated by TSMC. Key objectives for this project included: 1) the need to minimize die size to achieve cost targets; 2) a total power budget of under one watt and; 3) the need to deliver the completed design in the shortest time possible without comprising predictability or quality. The TN4010 device is now available from Tehuti Networks and is being fabricated by TSMC.

Implementation of the design was a joint effort between Tehuti Networks, a fabless semiconductor company located in Hertzliya, Israel and Uniquify, a provider of semiconductor design and implementation services based in Santa Clara, CA. The presentation will cover the basic approach that was used to design and implement the new device including how the tasks were divided up between the two companies to achieve the project objectives.

Another key aspect of the project that will be covered is the extensive use of IP in the design. The IP making up this design was sourced from Tehuti Networks, Uniquify, as well as from 3rd party IP suppliers. We will discuss the basic process of how the IP was chosen and qualified and how it helped the team to meet the project objectives.

Combining Design and IP to Deliver a Low Power / Low Cost 10GbE Controller



Agenda

- Company Backgrounds
- Design Challenges
- Project Overview
- Perseus
- Tehuti TN4010 Program
- Summary

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Company Backgrounds



- 10Gb Ethernet Traffic Accelerators
- Markets
 - SOHO servers
 - Office Servers and NAS
 - LAN-On-Mother (LOM) boards for high- mid-range desktop and entry level servers
 - Workstations, replacing "multi-1G" solutions
- Herzilya, Israel



- SoC design, IP and manufacturing services
- Markets
 - Communications
 - Networking
 - Mobile
 - Consumer
 - Wireless
 - Image processing
 - Storage
 - Medical
- Santa Clara, California

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Design Challenges



- Tehuti TN4010 design
- Required minimal die size for smallest possible footprint
 - Target area < 9mm²
- Achieve < 1 watt total power consumption
- Minimize turnaround time without sacrificing quality
 - Time-to-market essential
- Manufacture TN4010 device in TSMC 65nmG process
 - 65nmG process offers optimum size/performance/cost tradeoff
 - ~ 1M gates / 45 on-board memories / ~ 1.5M memory bits



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Project Overview

- RTL developed by Tehuti Networks
- IP qualified and sourced by Uniquify
- RTL-to-GDSII and IP integration implemented by Uniquify
- DFT insertion implemented by Uniquify
- Implementation process driven by Perseus™ design management system

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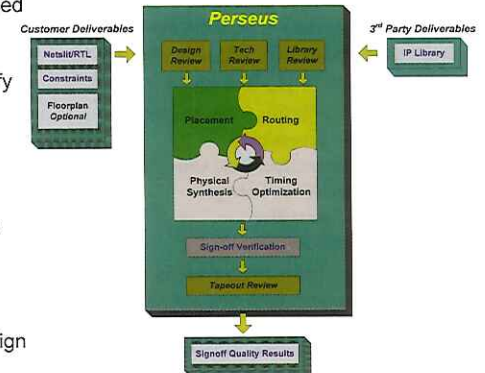
Perseus™

Automated SoC Design Management System

- Proprietary software system developed by Uniquify
- Used on all SoC programs at Uniquify

Key benefits

- Comprehensive design analysis identifies issues at project start
 - Independent of EDA tools – analysis runs directly on netlist and library
 - Reduces time, effort and resources required to achieve tapeout
- Deterministic flow leads to rapid design closure convergence
- Dynamic project monitoring allows optimal deployment of resources

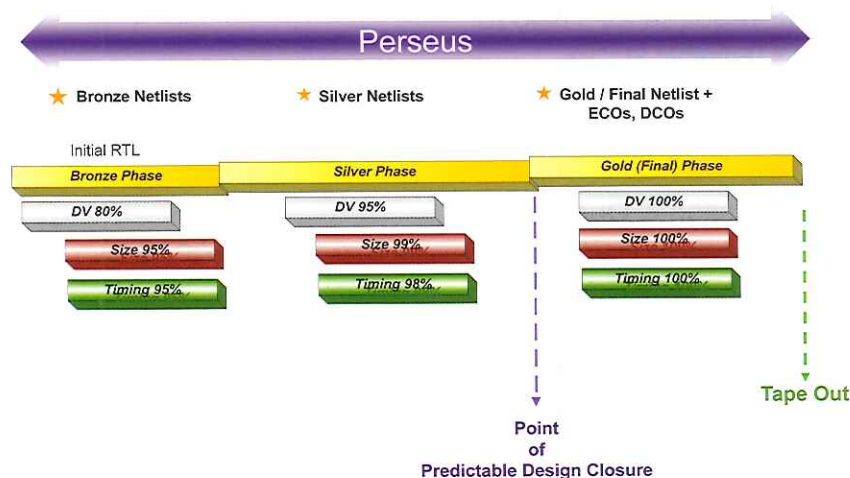


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Process Steps



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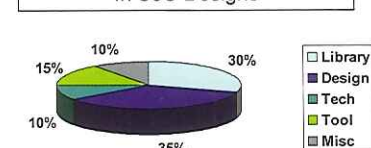
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Early Review is Critical

- Early review identifies issues that may be very tough to solve during implementation
 - Reduces schedule risk
 - Reduces resource costs

Sources of Implementation Issues In SoC Designs



- Perseus – thorough reviews at project start:
 - Library review
 - Tech review
 - Design review

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Library Review



- Regression based library clean up
 - Test case generation
 - Exercises entire ASIC flow
- Basic sanity/consistency checks
 - LEF vs. LIB & Verilog vs. CDL
- Physical library review items
 - Pin accessibility
 - Power/Ground pin structure
 - Route/via blockages
 - Power issues
 - DRC/LVS/ANT
- Timing library review items
 - Buffer/Inverter Characterization for Optimization
 - Max transition/capacitance
 - SDC/Timing script check

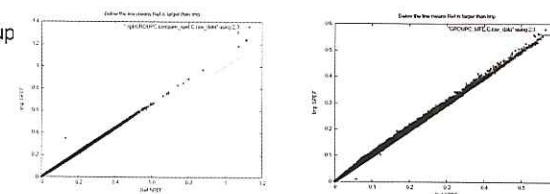
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Tech Review



- QoR of EDA tools highly dependent on accuracy of tech files
 - Inaccurate tech files lead to correlation problems
 - Cannot be too conservative or too optimistic
- Major tech files are reviewed
 - P&R technology files
 - Parasitic extraction stack-up
 - DRC/LVS/ANT decks

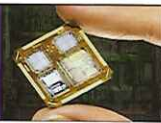


Extraction correlation between implementation and Sign-off extraction tools

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Design Review



- RTL cleanup
 - Syntax and coding style check
 - LINT check
 - Synthesis warnings
- SDC cleanup
 - Clock statement check
 - Unconstrained sequential elements
 - Unconstrained endpoints
 - Unconstrained input and output ports
 - Timing exception
 - Budgetary condition check
 - Timing loops
- DFT cleanup
 - Clock violations
 - Clock to data violations
 - Reset violations
- Gate-level netlist analysis
 - Clock network analysis
 - Reset network analysis
 - High-fanout net identification and analysis
 - Logical hierarchy / partitioning
 - "assign" statement
 - Spare gate analysis
- Floor plan Information
 - Pin assignment
 - Macro block placement / connectivity
 - Power budget / planning

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IP Selection – TN4010



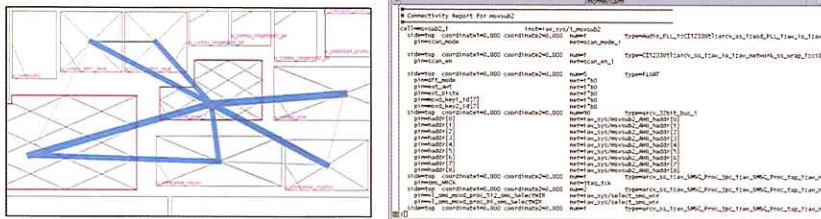
- IP required for TN4010
 - Ethernet SerDes
 - PCIe SerDes (required GEN2)
 - PLL
- Selection & Qualification
 - Driven by previous use experience (e.g. "known IP quality")
 - Cost considerations
- IP sourced from two third-party IP vendors
 - Uniquify managed sourcing and integration of IP – reduced integration risk

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Minimize Die Size

- Perseus used to do “what-if” floorplanning analysis
 - Target die size < 9mm²
- Block placement
 - Considers primary I/O interface and inter-block connections
 - GUI-based fly-line display shows global connection view
 - Perseus performs comprehensive connectivity analysis to provide detailed view

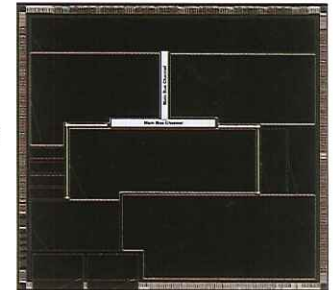


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Minimize Die Size

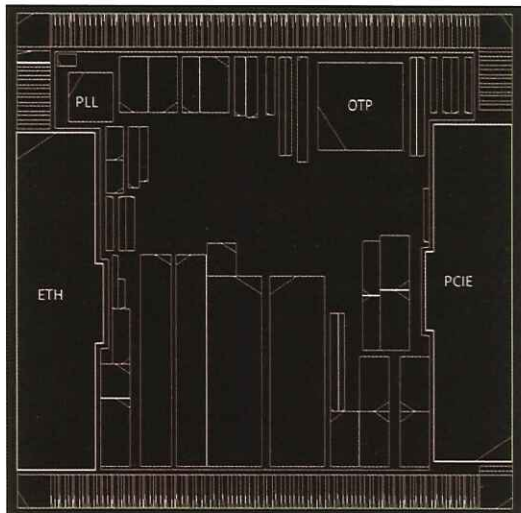
- Block pin assignment and optimization
 - Perseus gives users guidance on how to assign block-level pins
- Global net planning
 - Perseus automates global net buffering process to attain the best possible delay
- Channel planning
 - Perseus reserves enough channel width where more routing resources are required
 - Utilizes rectilinear floorplan to minimize “dead” area



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Tehuti TN4010 Floor Plan



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Achieving Power Goal

- TN4010 was designed to achieve lowest possible power
 - Target total power < 1W
 - Tehuti RTL was already optimized for low power operation
- Perseus derived additional power optimization via
 - Dynamic power analysis with decoupling cap cell insertion
 - Peak current sensitive area decoupling cap cell insertion
 - Around power sensitive area such as memories
 - Area based decoupling cap insertion
- Final silicon achieved ~ 0.9W total power

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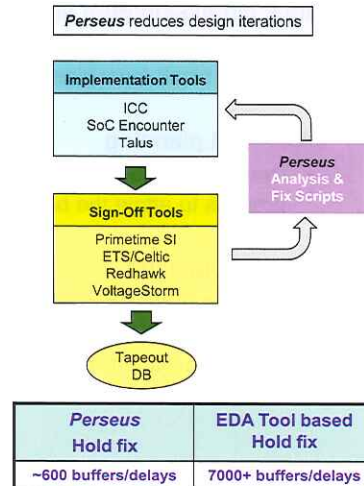
Design Closure

- Perseus flow supports seamless integration between sign-off tools and physical implementation tools

- Setup and hold violations
- Transition violations
- Max capacitance violations
- Signal integrity violations
- Antenna violations

- Allowed rapid convergence to design closure

- Final RTL to tape out in less than 2 weeks



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Tehuti TN4010 Summary

- Design objectives met
 - Die size: target area < 9mm² achieved
 - Total power: ~ 0.9W
 - Project turnaround time of 2 months from project start to tapeout
- Early Perseus analysis and planning reduced final RTL to tape out to 2 weeks!



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Summary

- IP
 - Single point for qualification, procurement and management
 - Reduced both integration and schedule risk
- Perseus
 - Up-front independent design analysis eliminates surprises during SoC implementation
 - Deterministic / convergent flow drives to rapid closure
- Tehuti TN4010
 - Perseus flow delivered final RTL to tape out in only 2 weeks
 - Device achieved area, power and performance goals

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